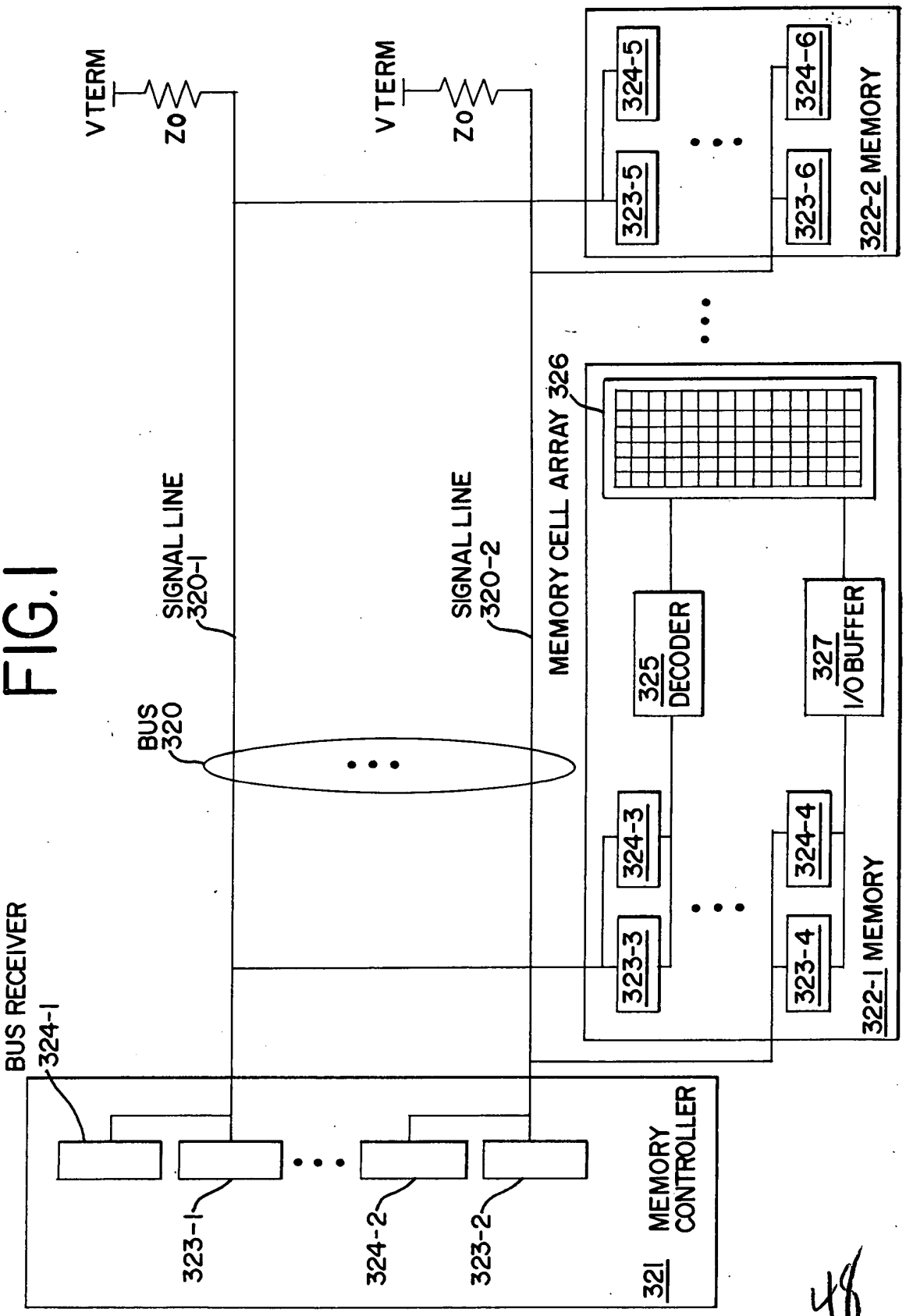
FIG. 1



48

FIG.2

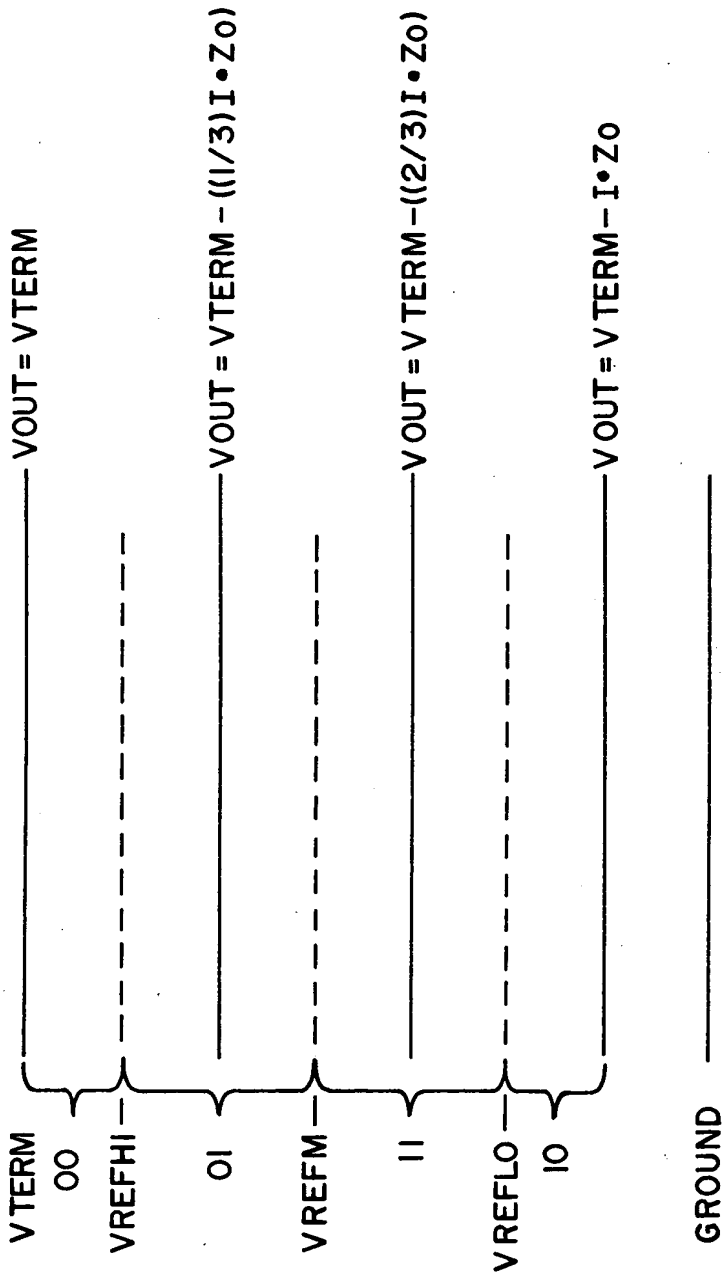


FIG.3A

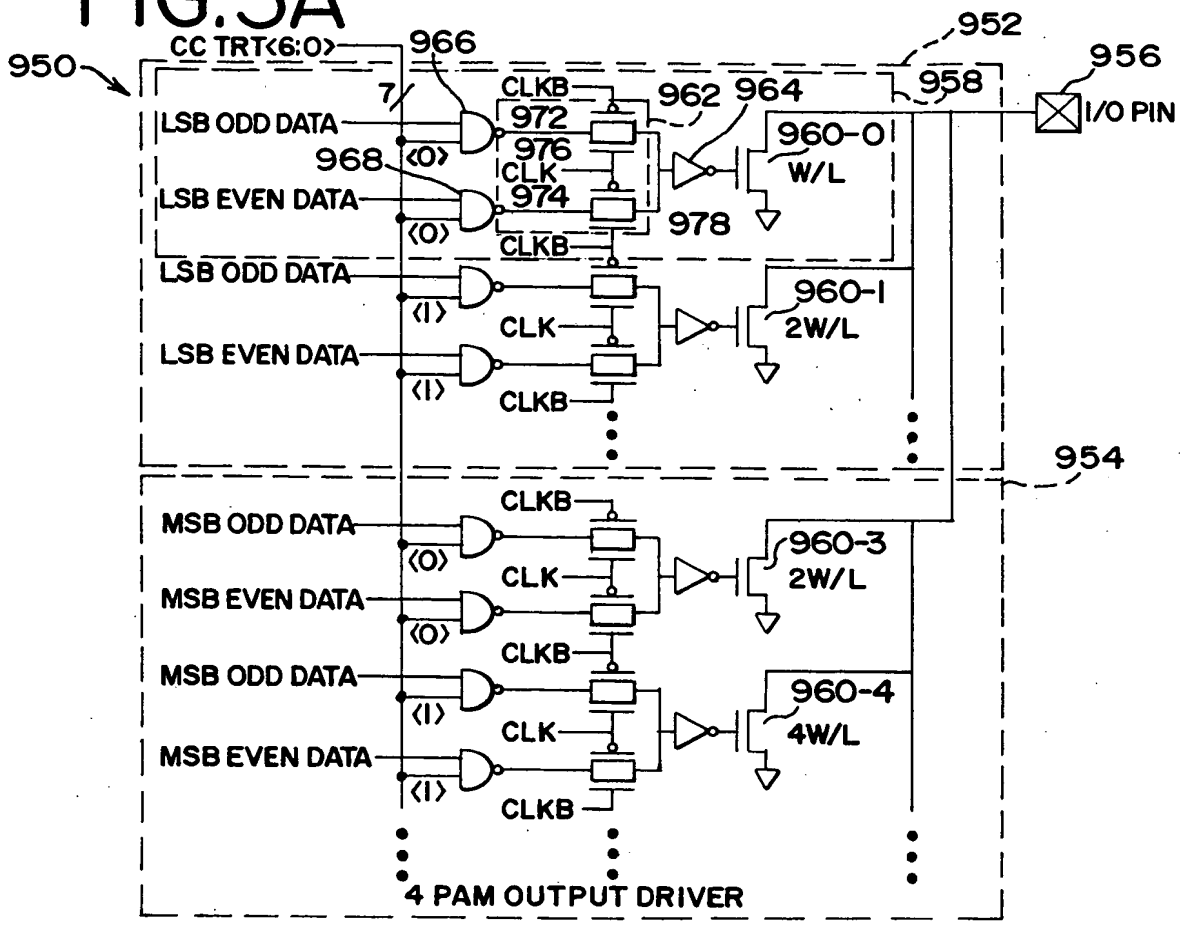


FIG.3B

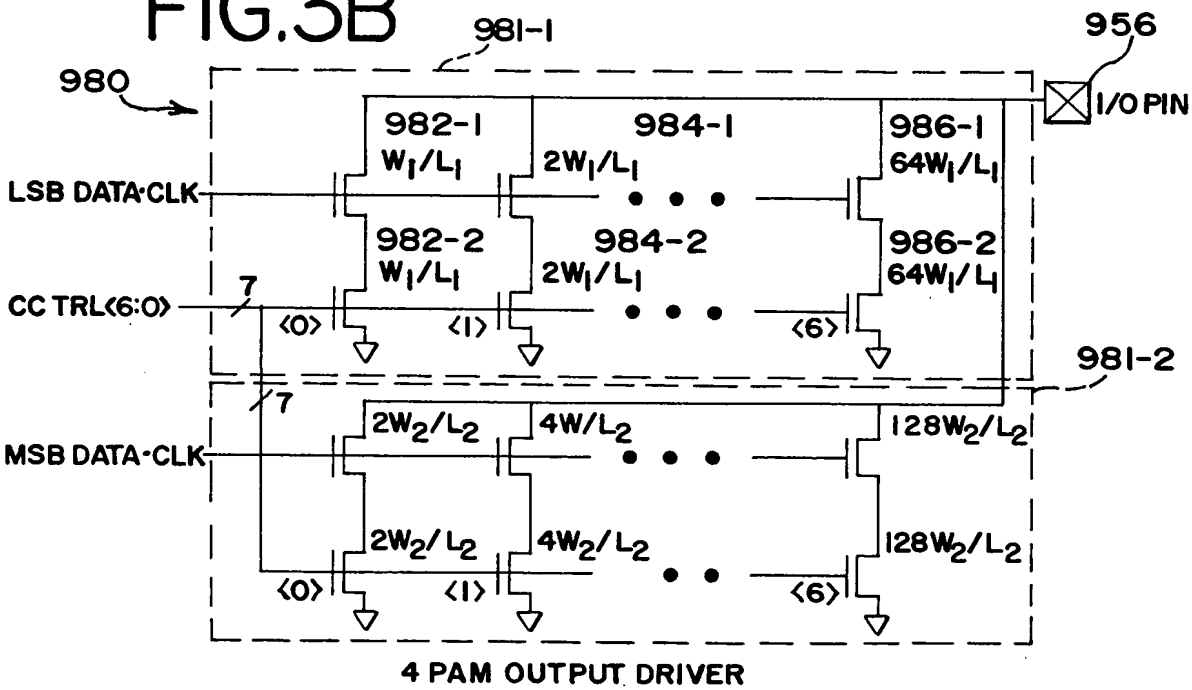


FIG. 4A

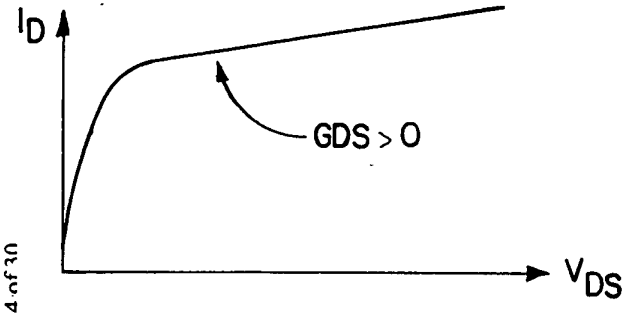


FIG. 4B

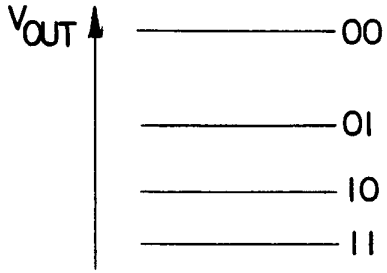


FIG. 4C

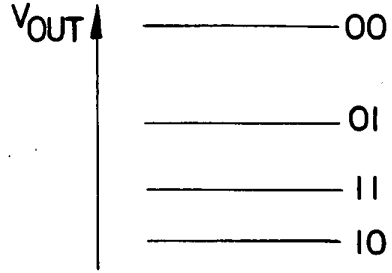


FIG.5A

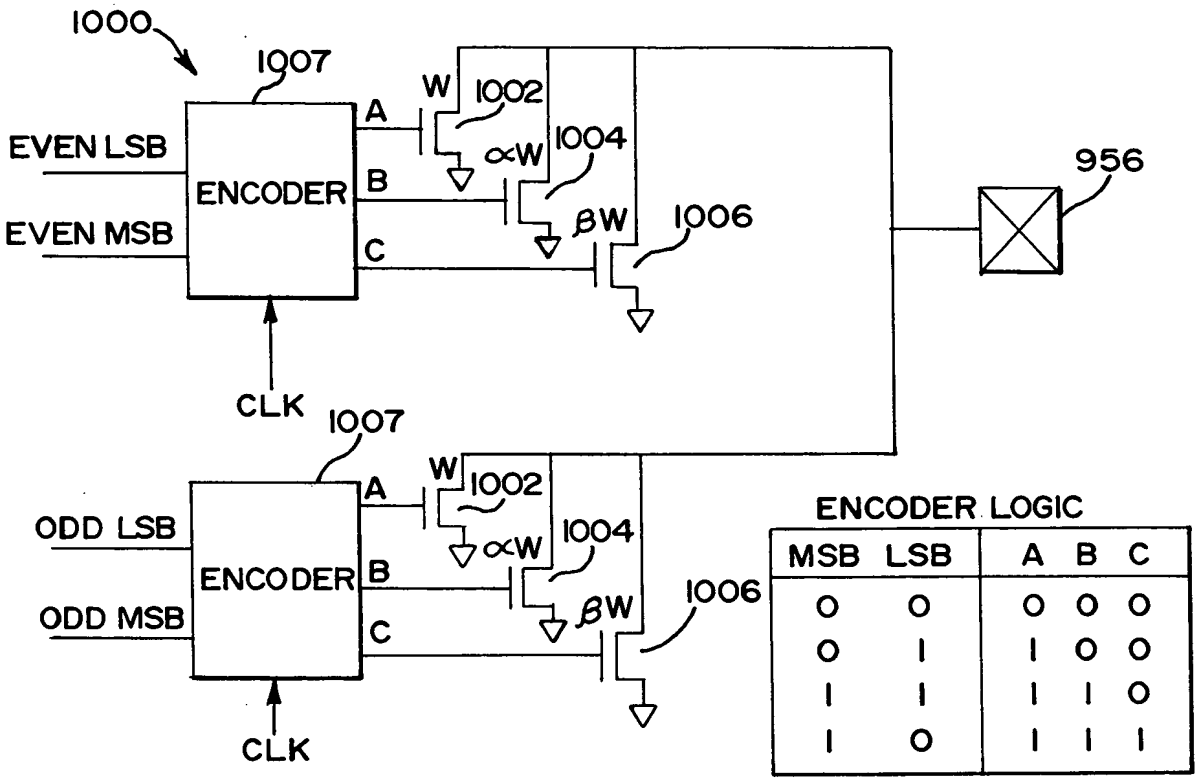


FIG.5B

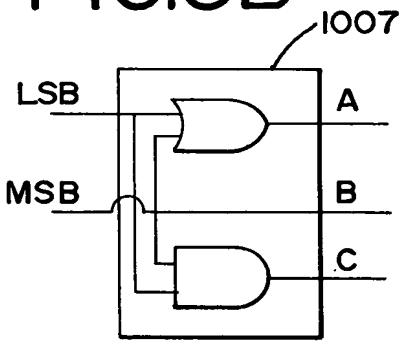


FIG.5C

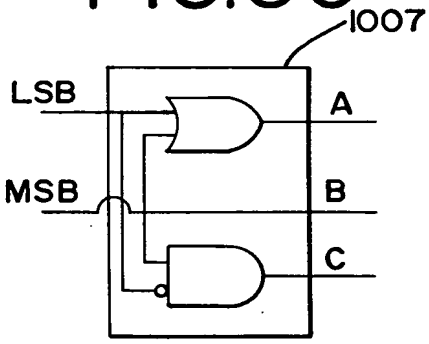
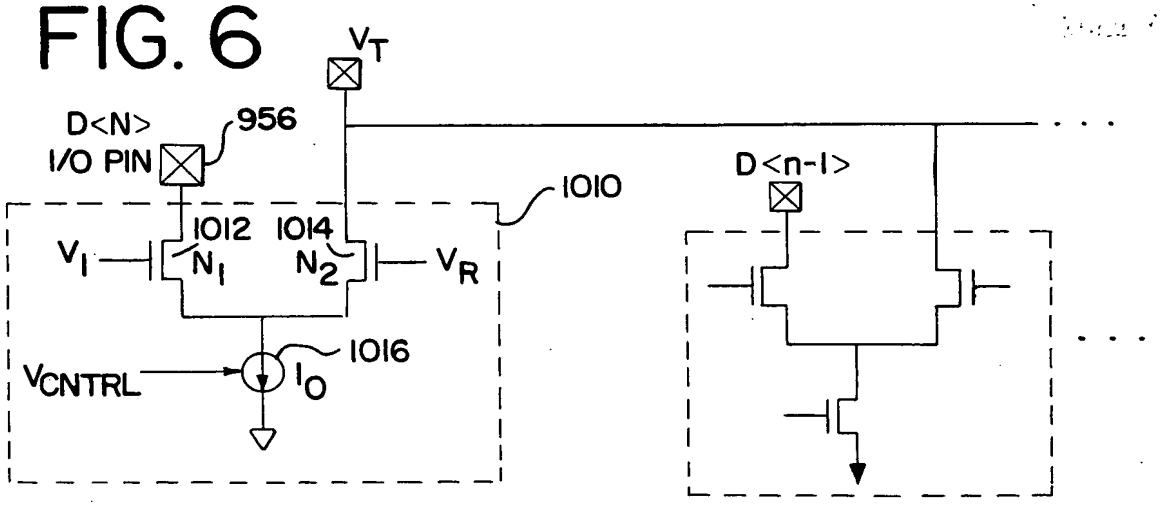


FIG. 6



CIRCUIT TO REDUCE SWITCHING NOISE

FIG. 7

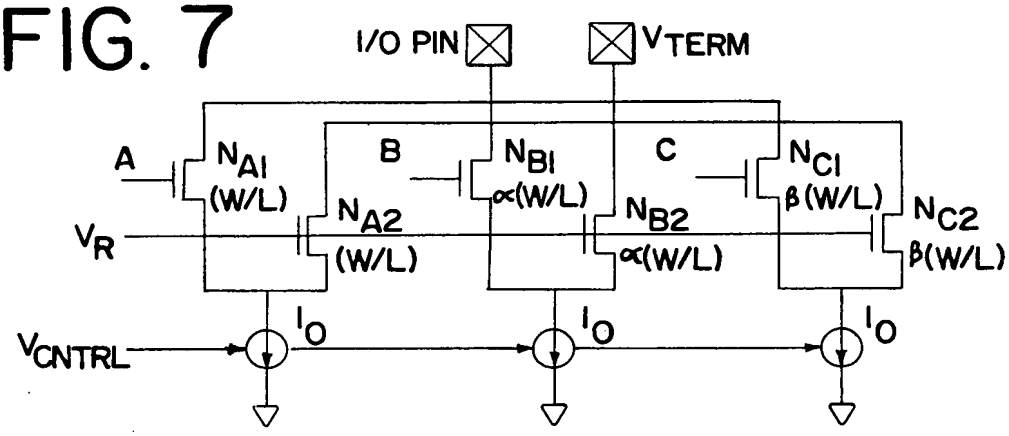
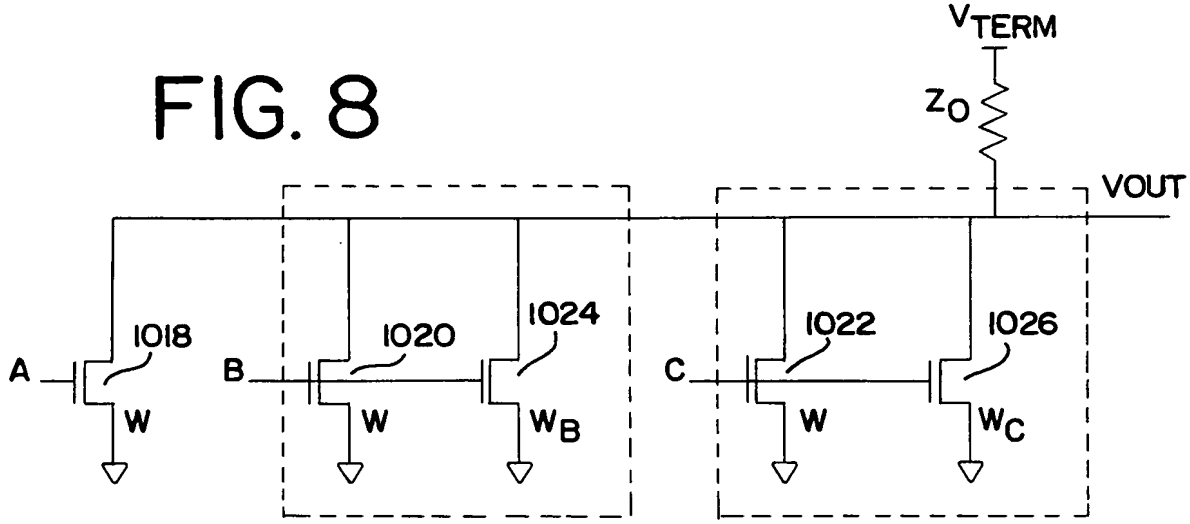
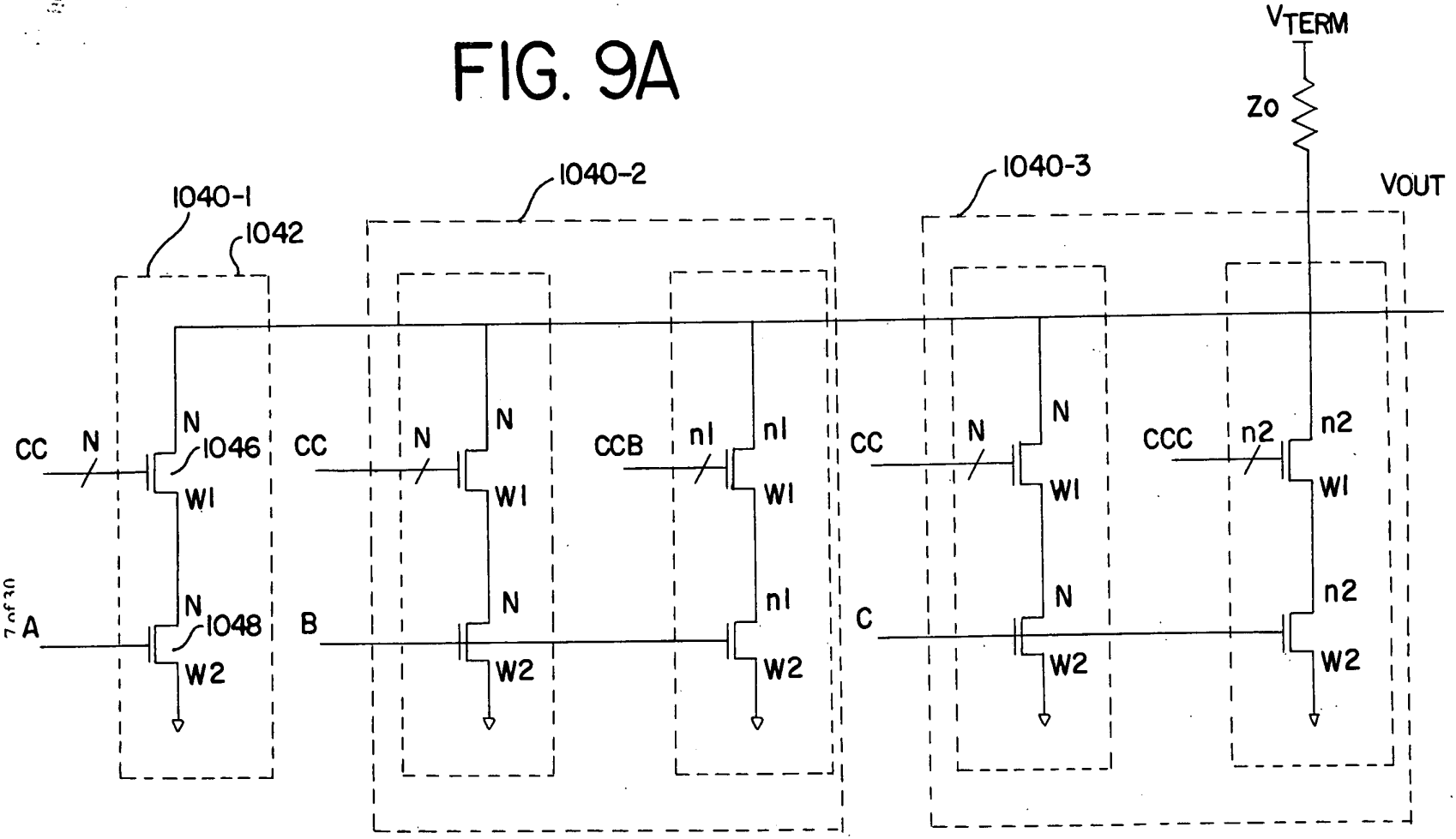


FIG. 8



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER

FIG. 9A



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 9B

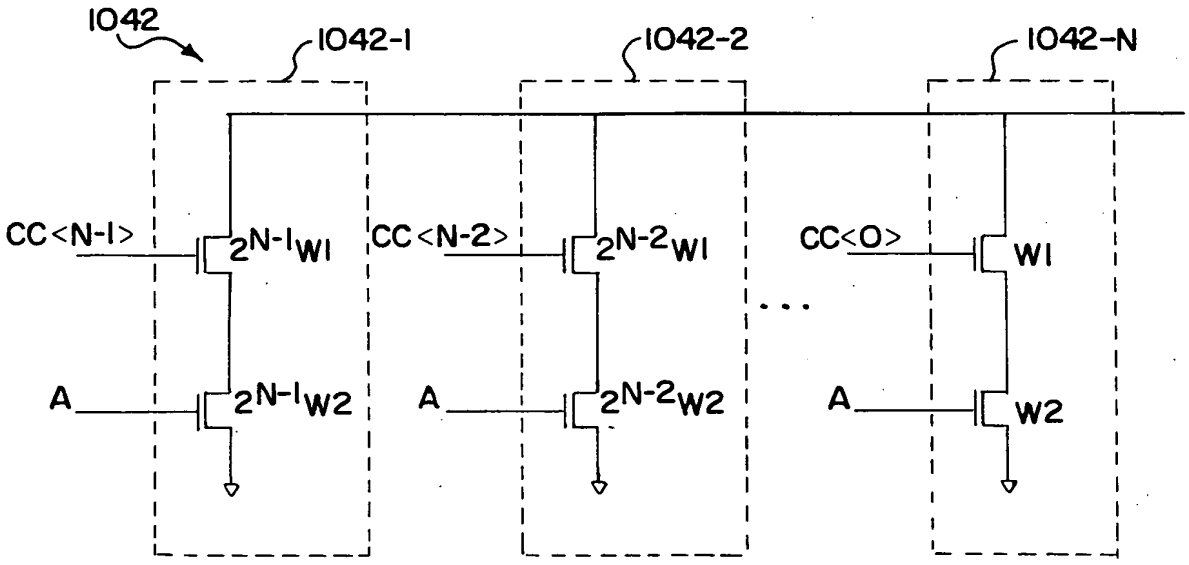


FIG. 9C

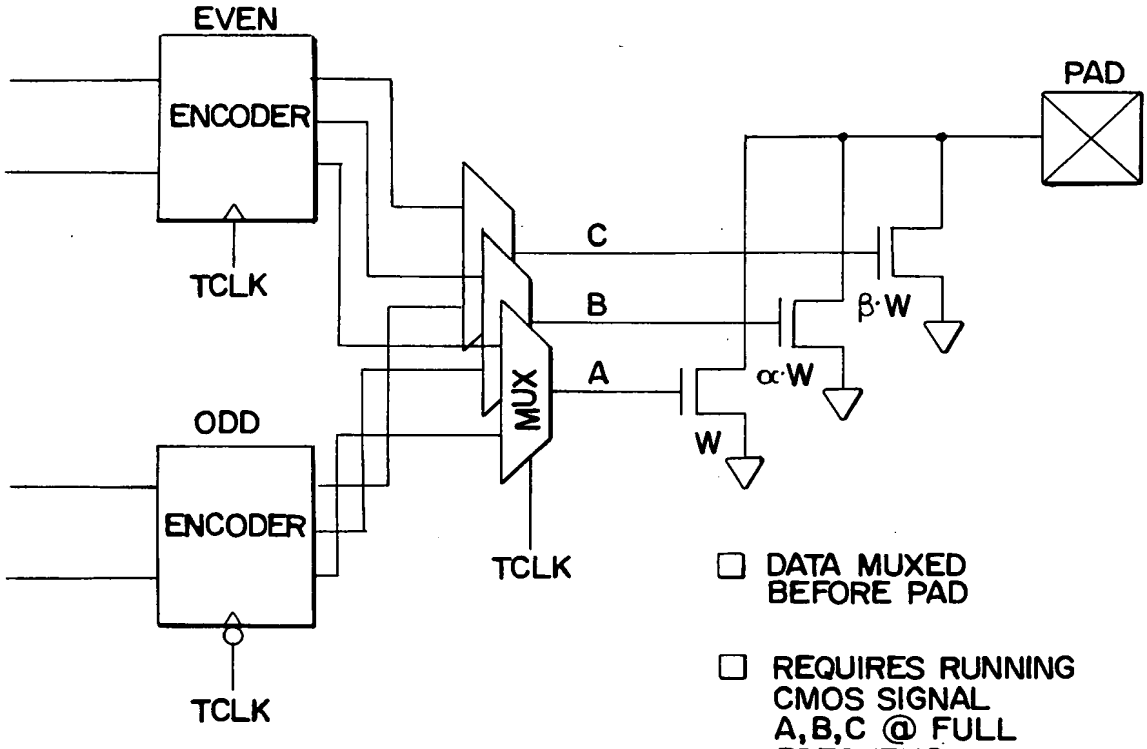
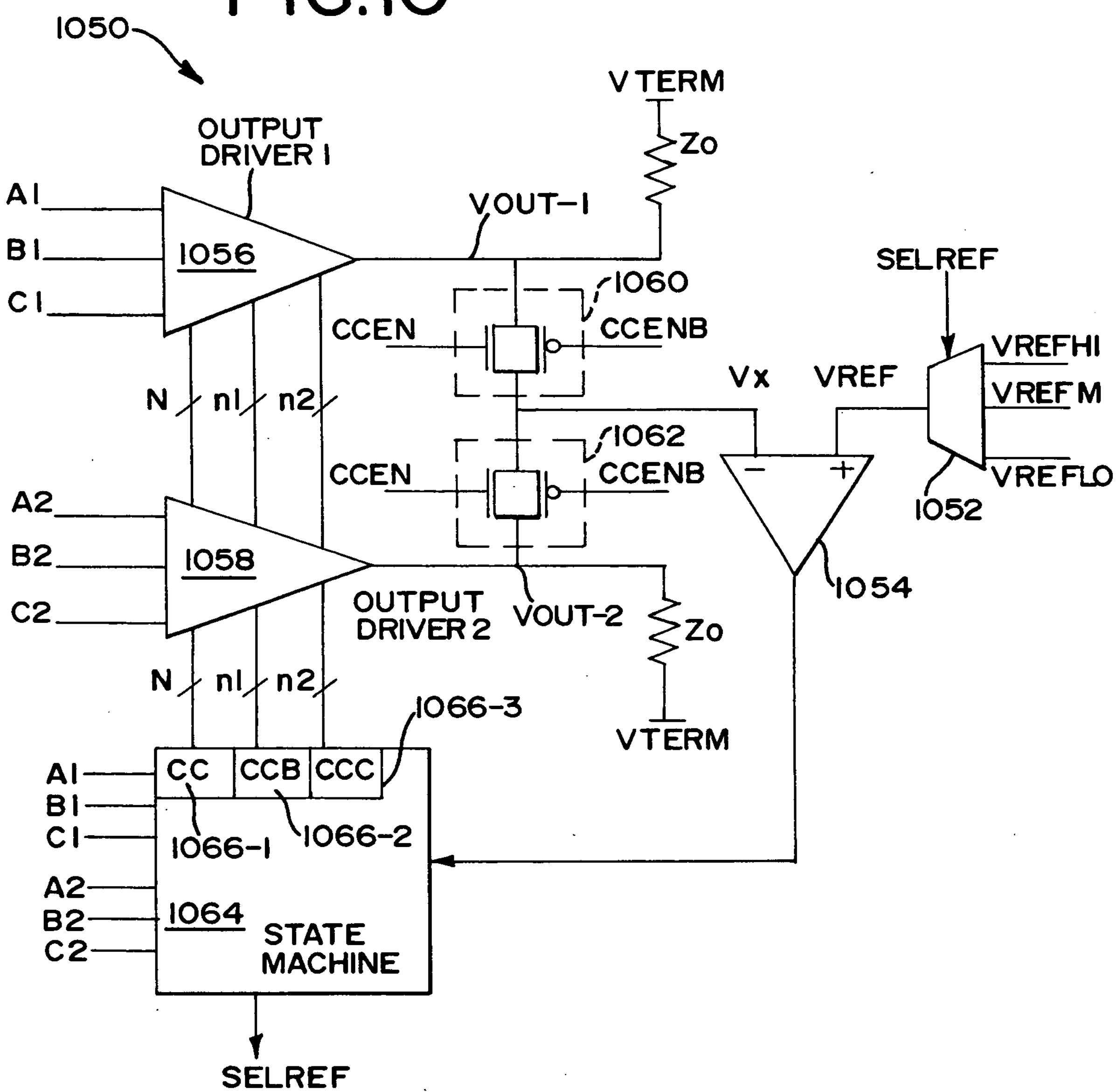
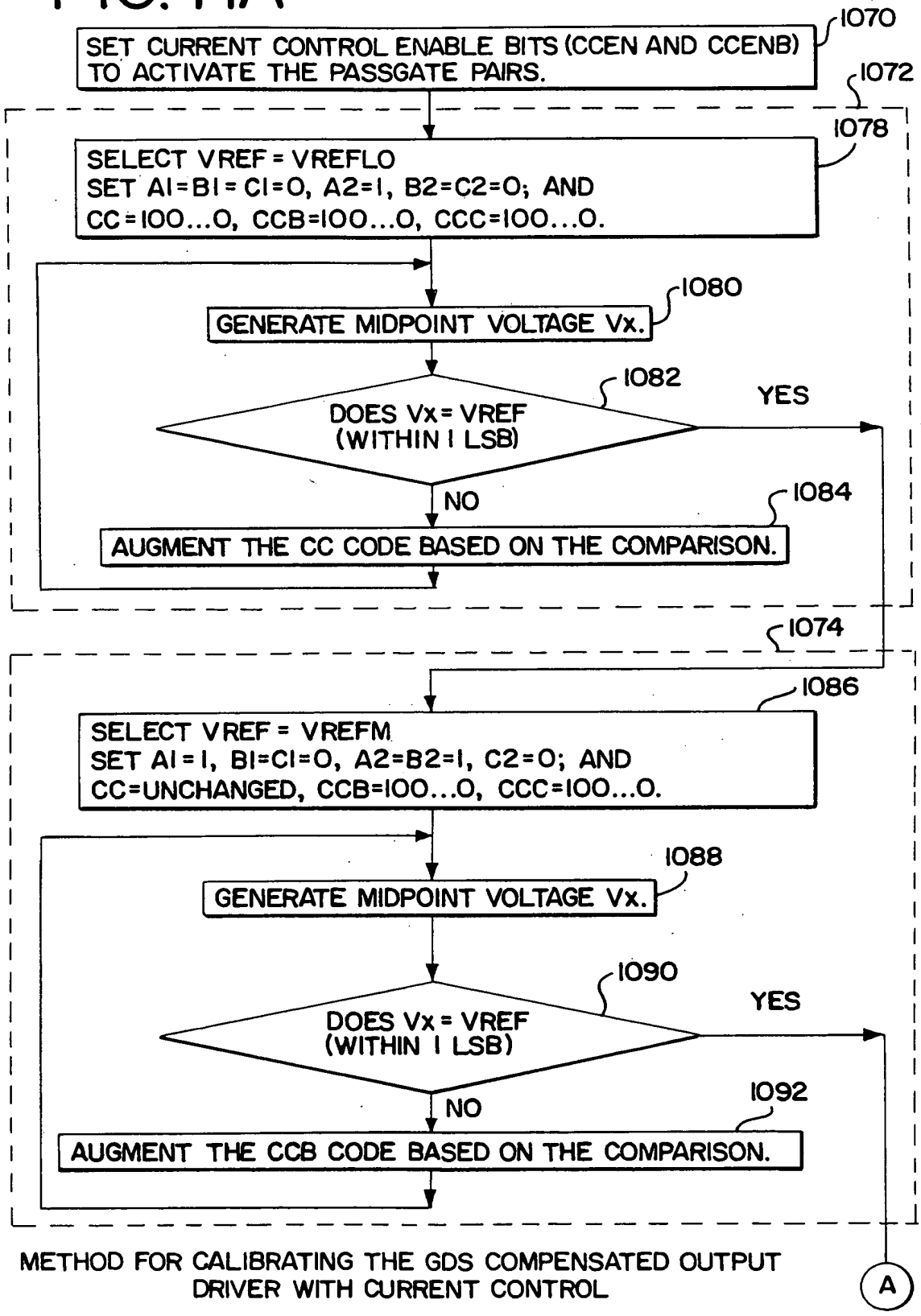


FIG. 10



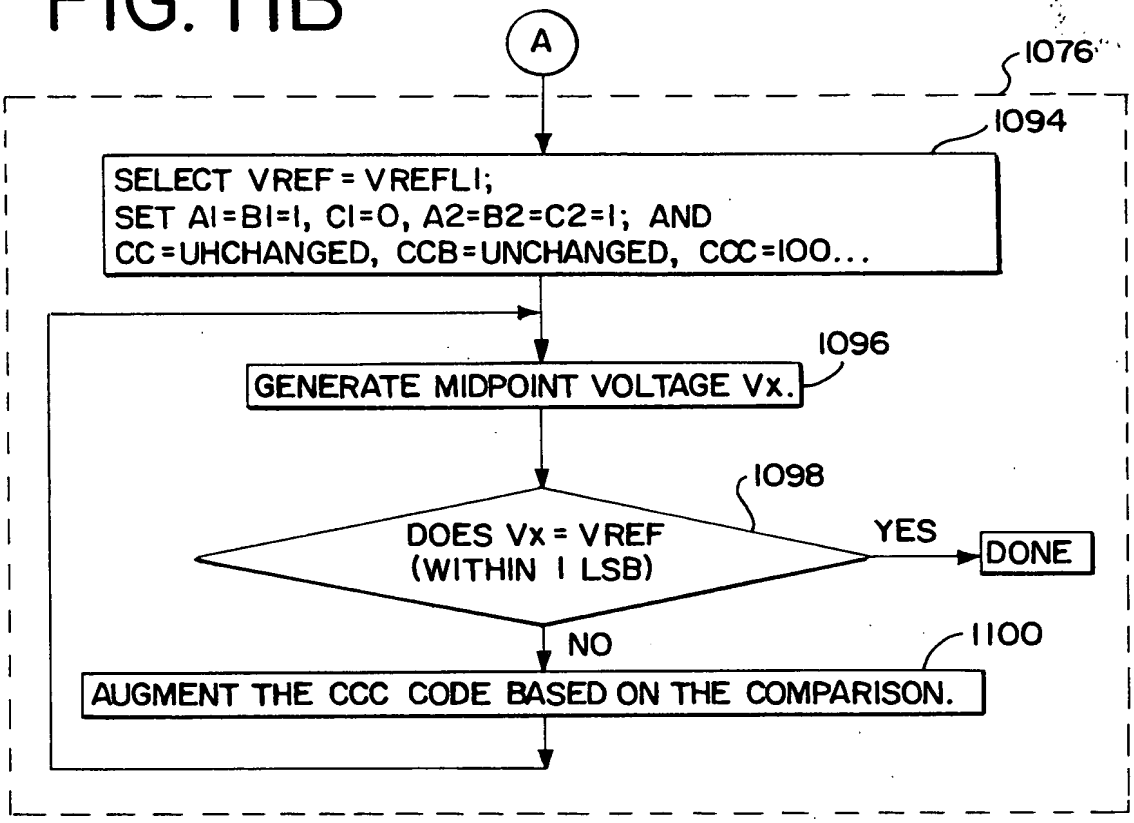
CIRCUIT FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11A



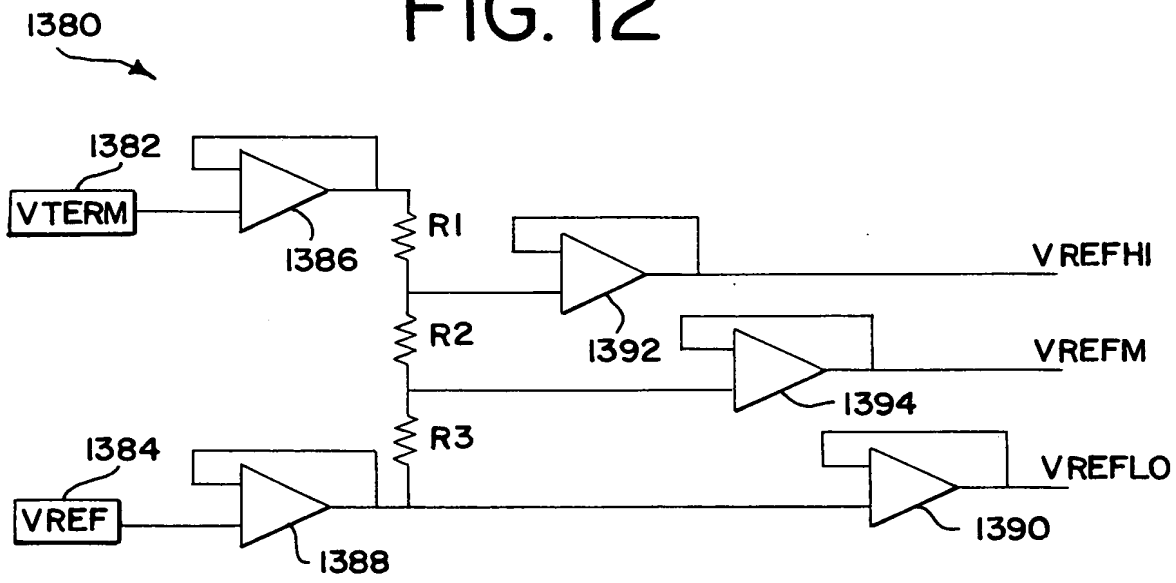
METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11B



METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 12



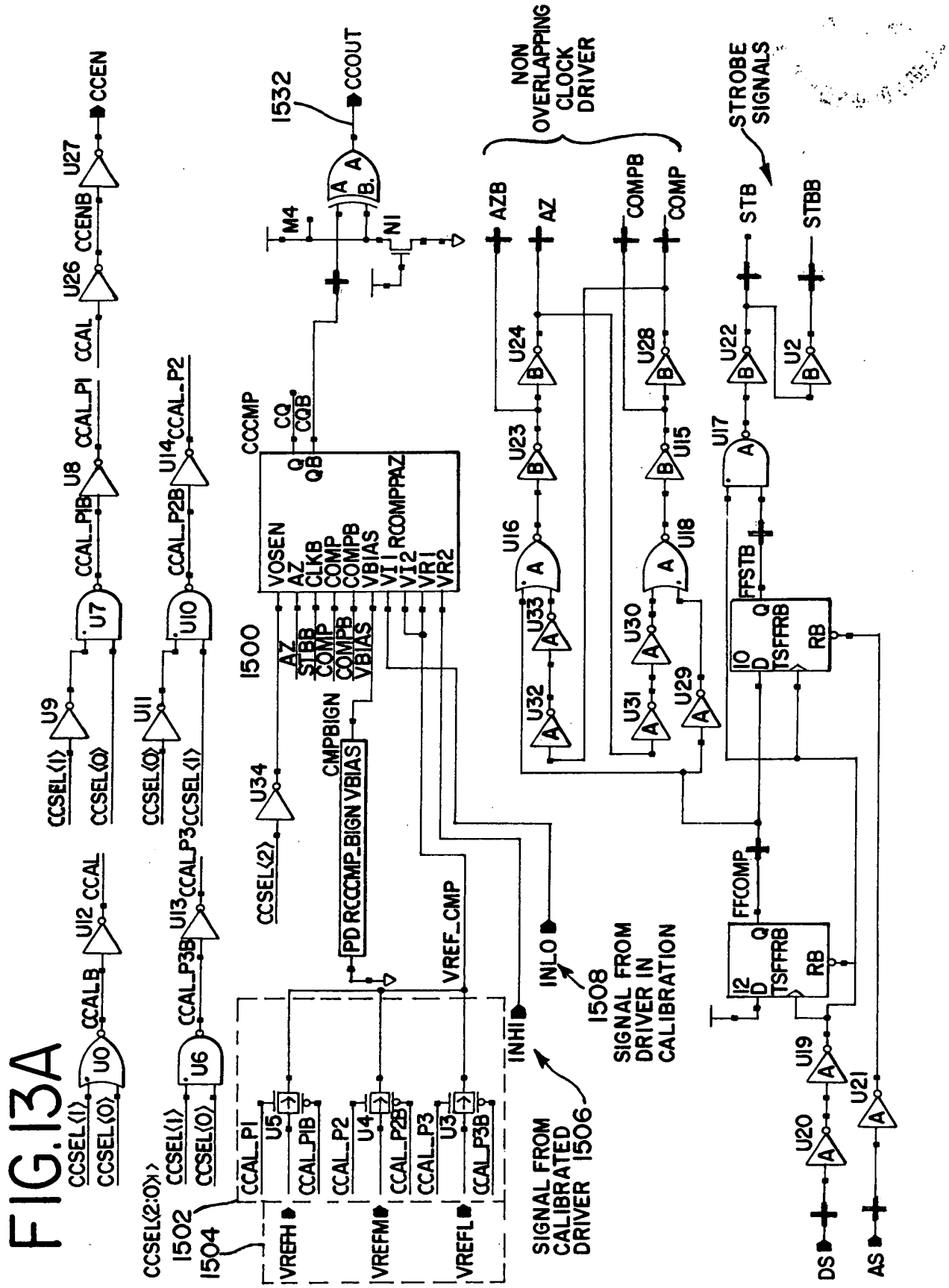


FIG.13A

FIG.13B

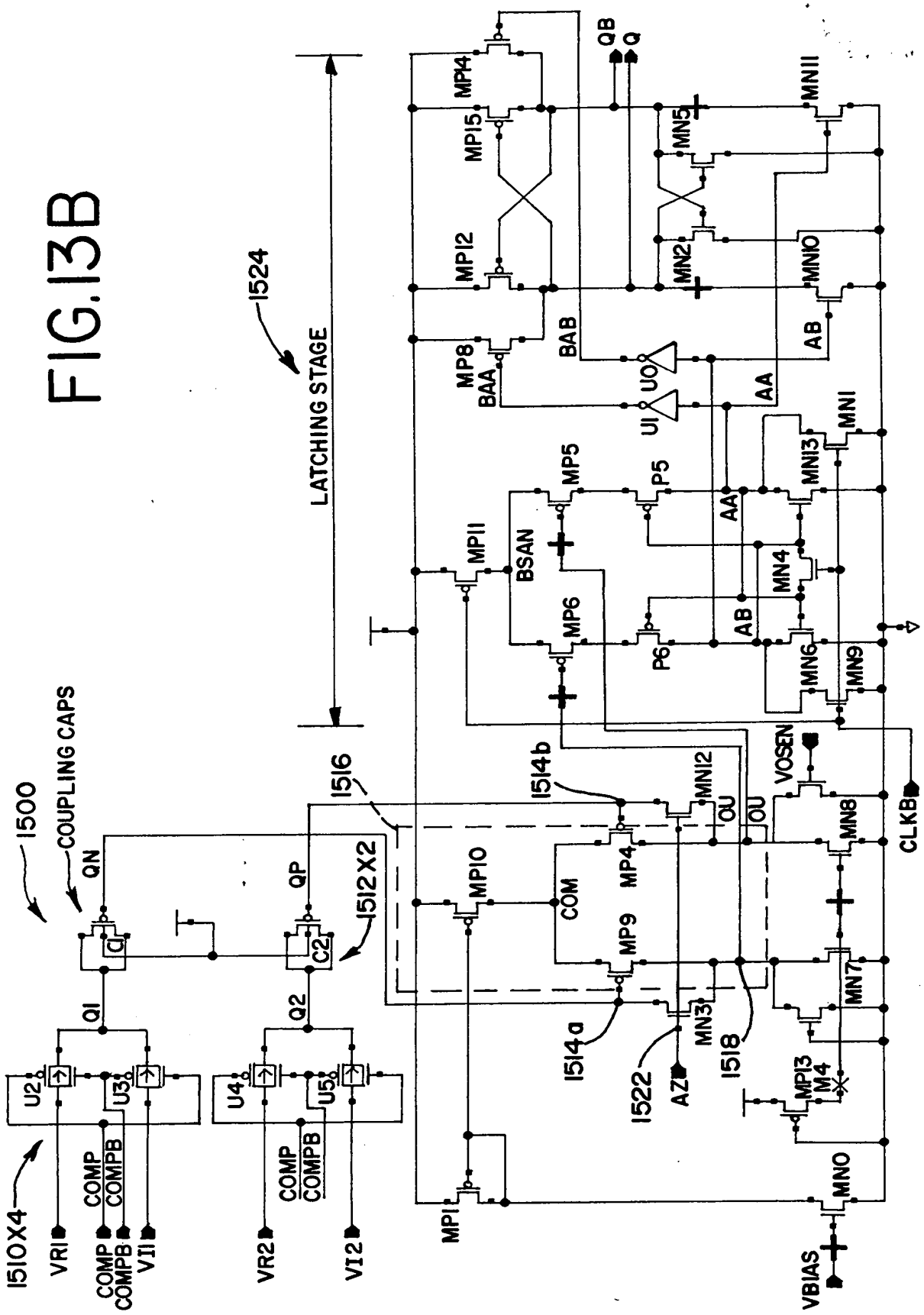
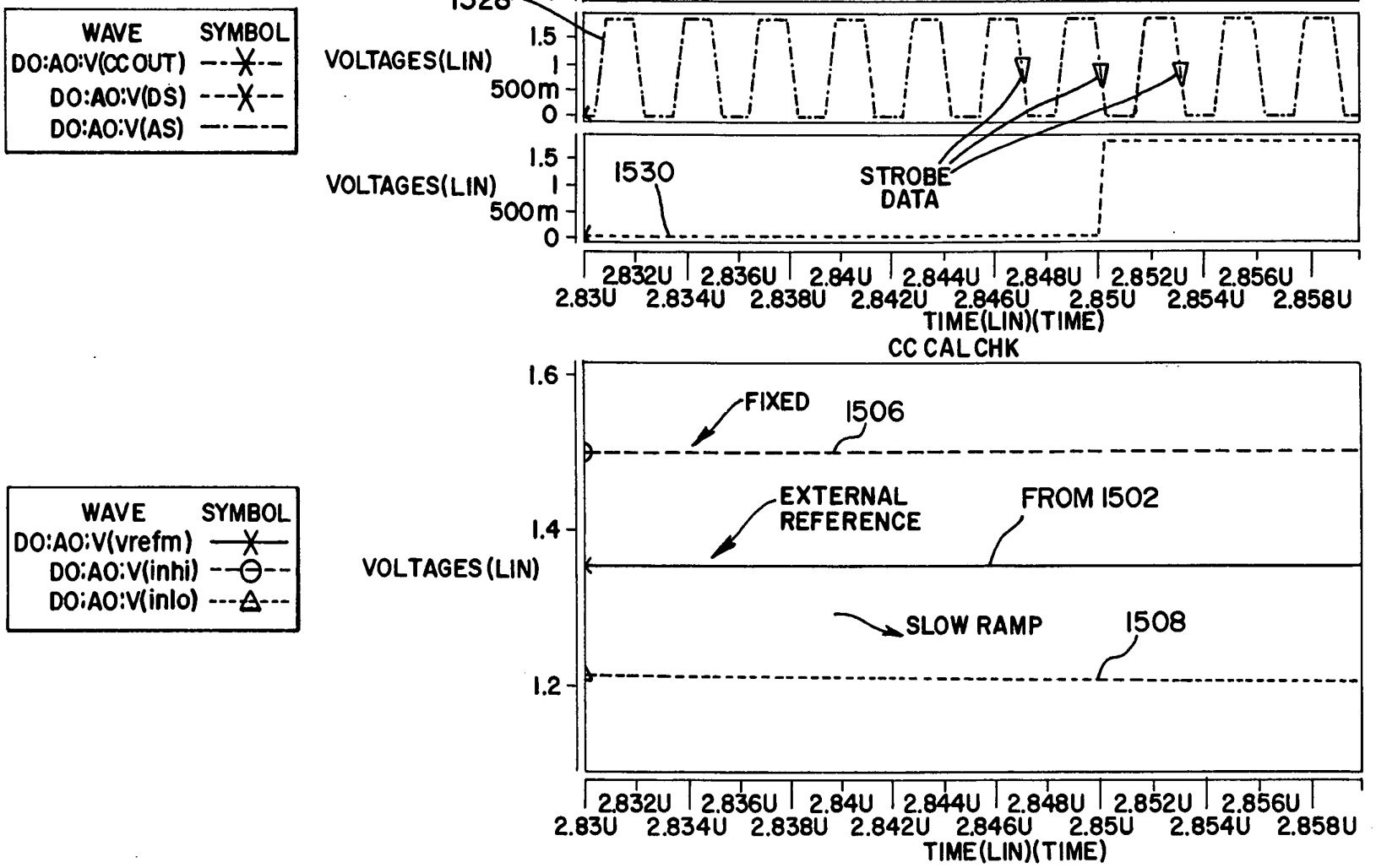


FIG.13C



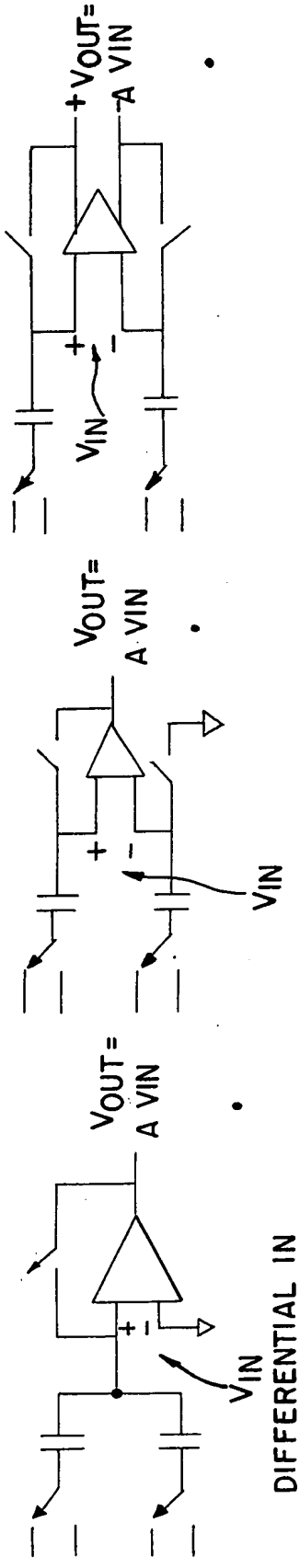


FIG. 13D

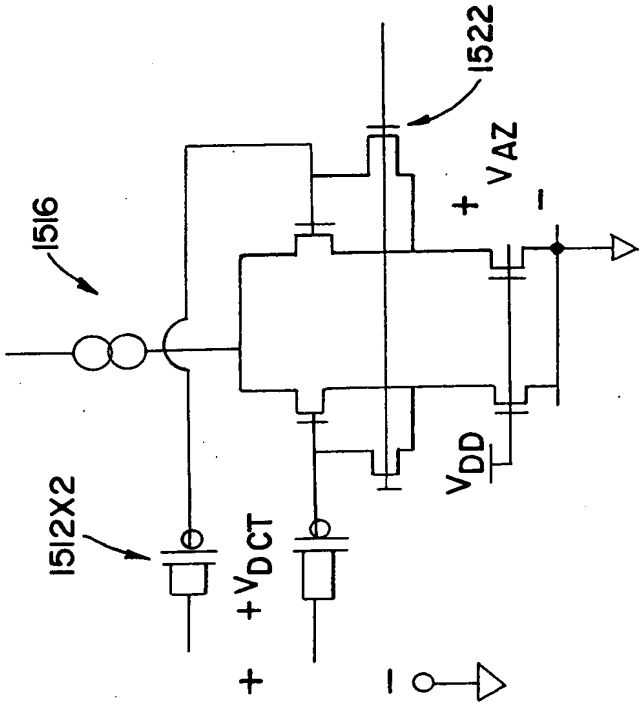
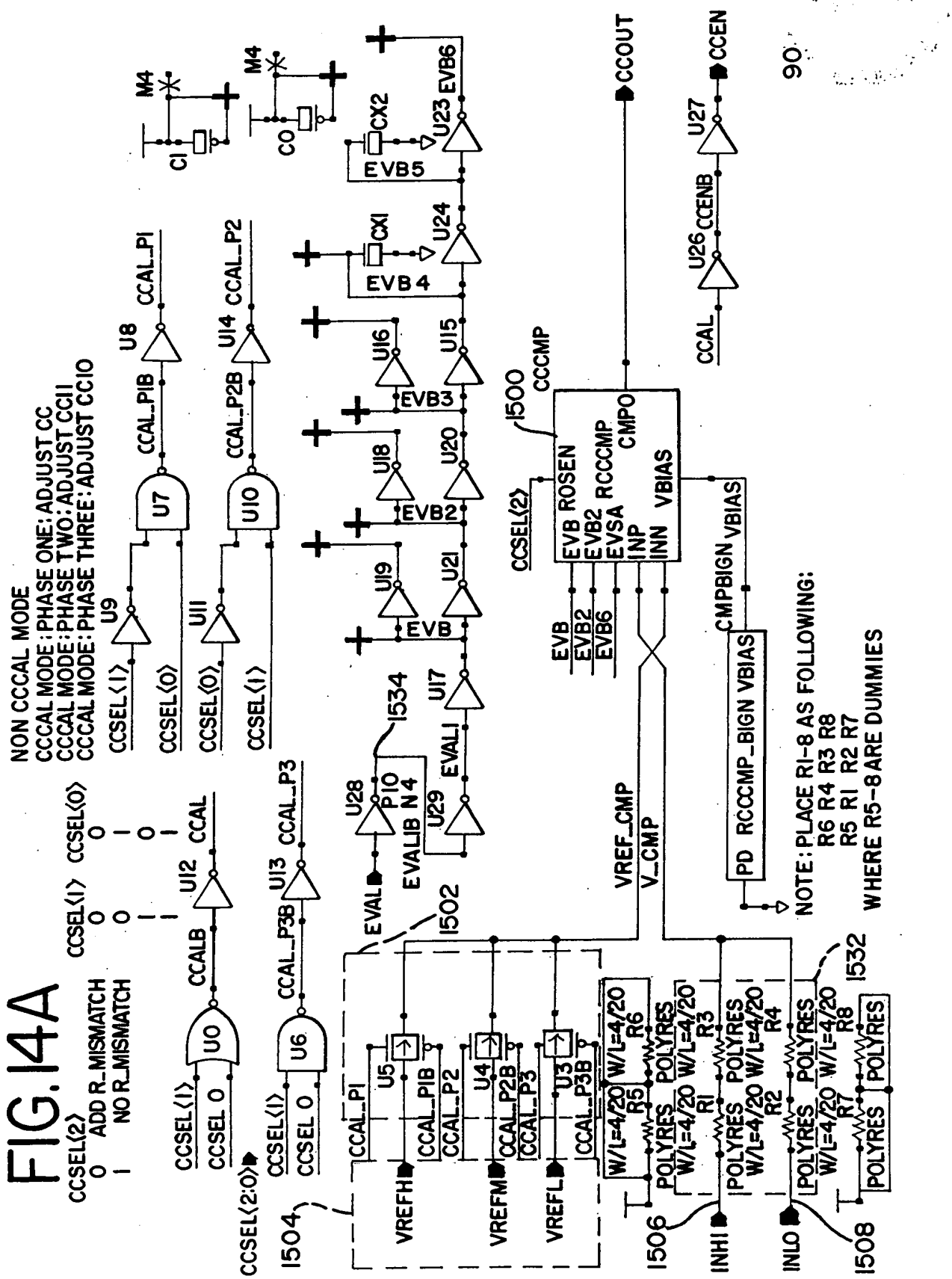


FIG. 13E



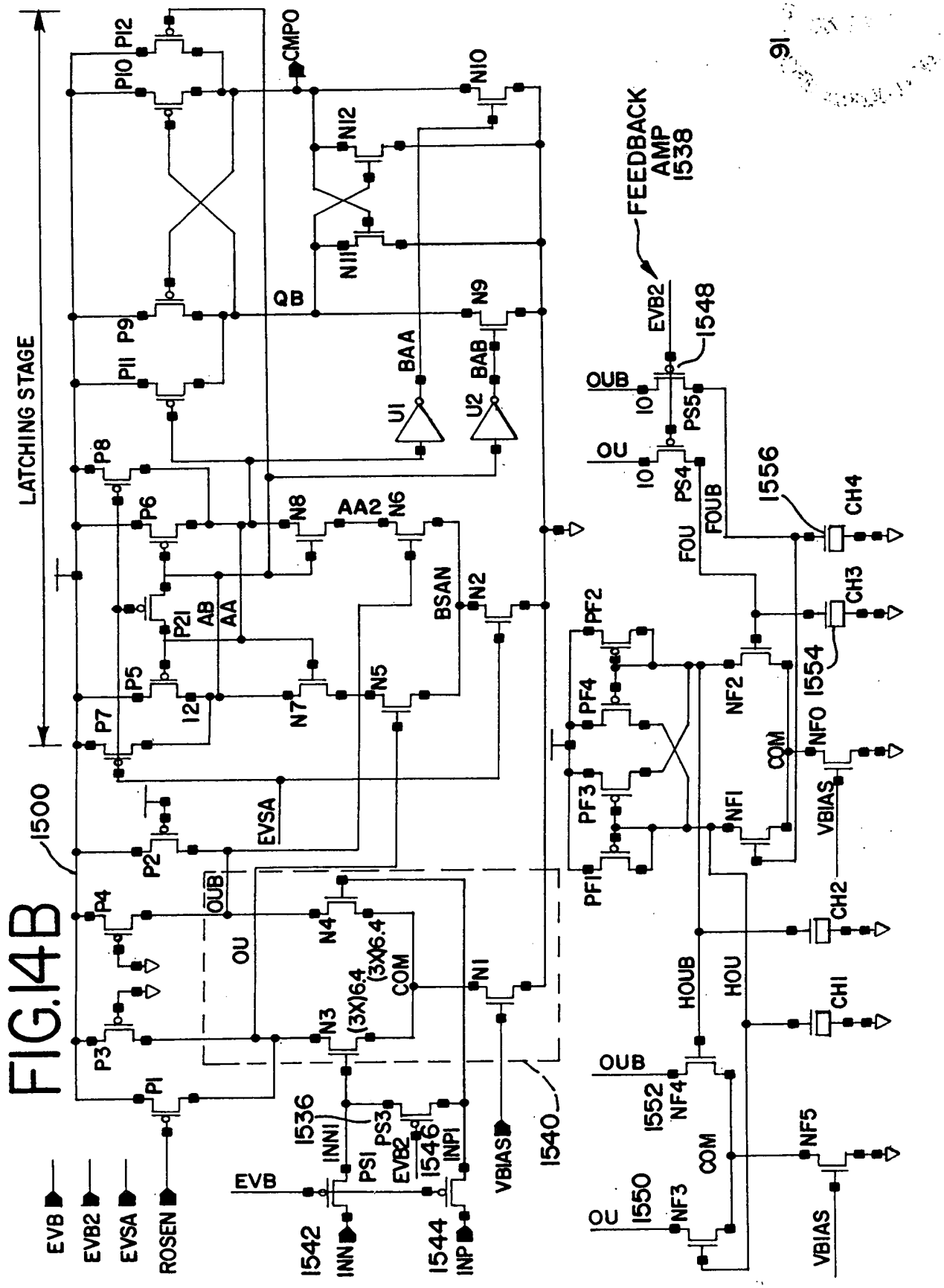


FIG.14B

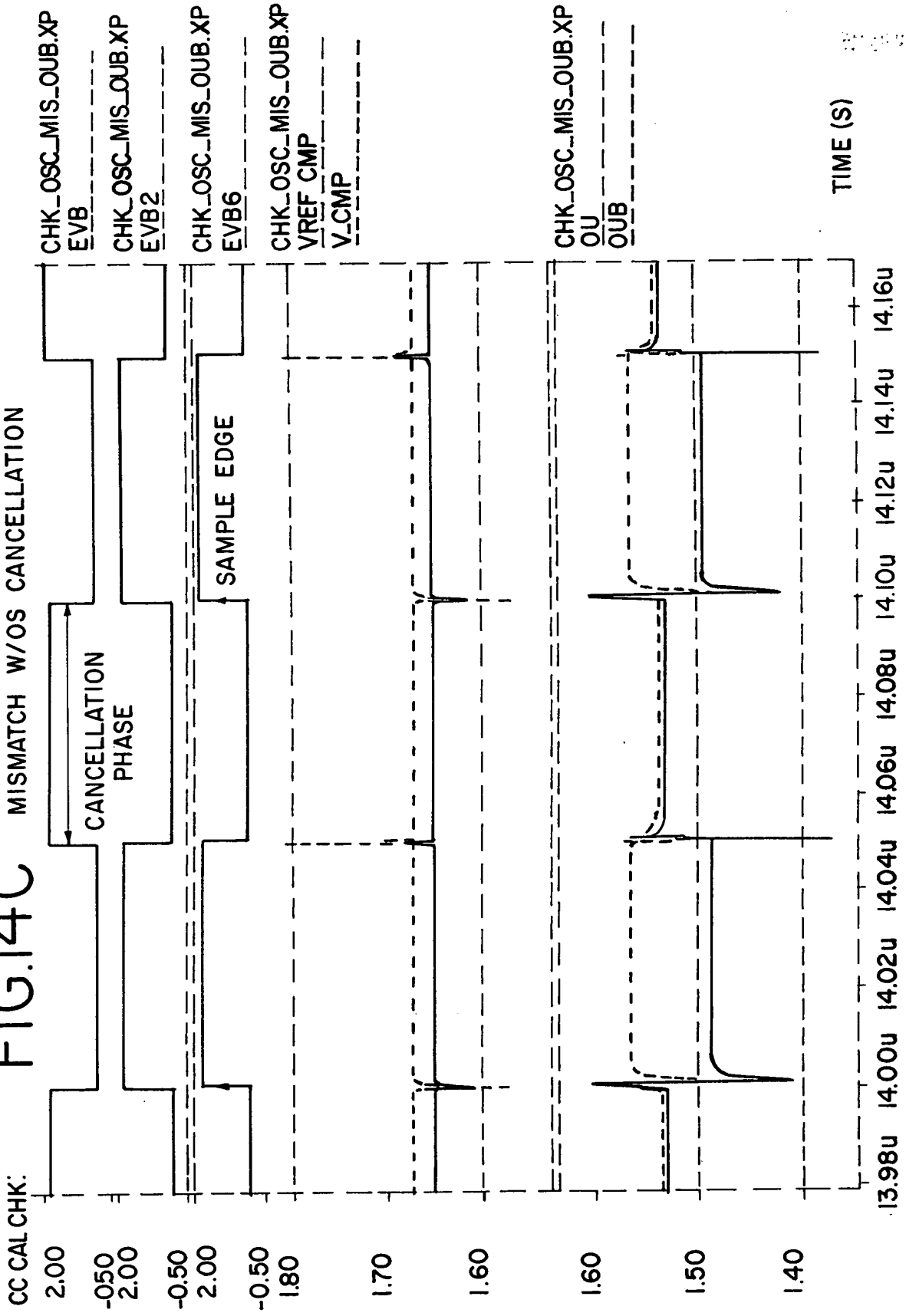

CHK_OSC_MIS_OUB.XP
EVB
CHK_OSC_MIS_OUB.XP
EVB2
CHK_OSC_MIS_OUB.XP
EVB6
CHK_OSC_MIS_OUB.XP
VREF CMP
V_CMP
CHK_OSC_MIS_OUB.XP
OU
OUB
TIME (S)
MISMATCH W/OS CANCELLATION
CANCELLATION PHASE
SAMPLE EDGE
CC CAL CHK:
2.00
-050
2.00
-0.50
2.00
-0.50
1.80
1.70
1.60
1.60
1.50
1.40
13.98u
14.00u
14.02u
14.04u
14.06u
14.08u
14.10u
14.12u
14.14u
14.16u

FIG.14C

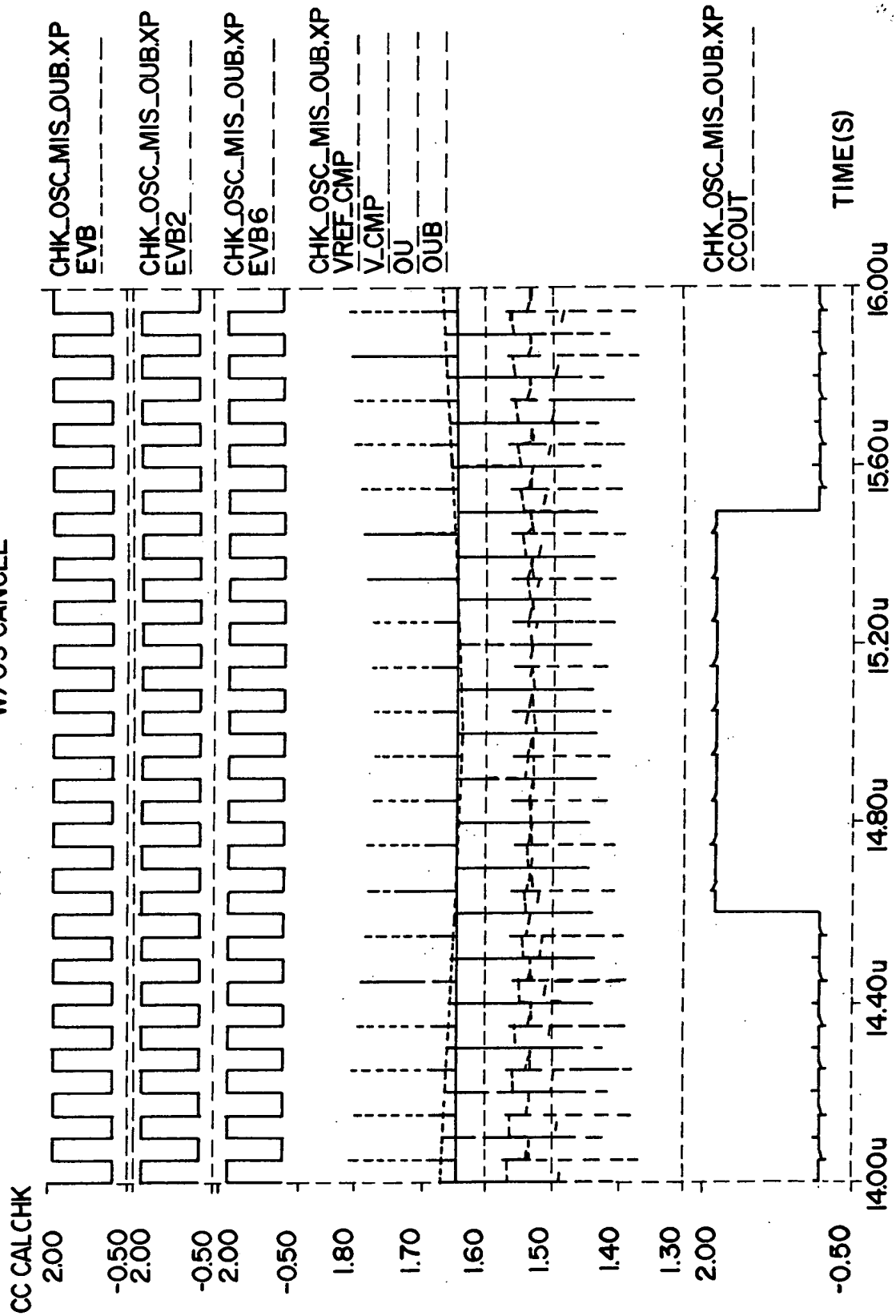


FIG.14D

FIG.15A

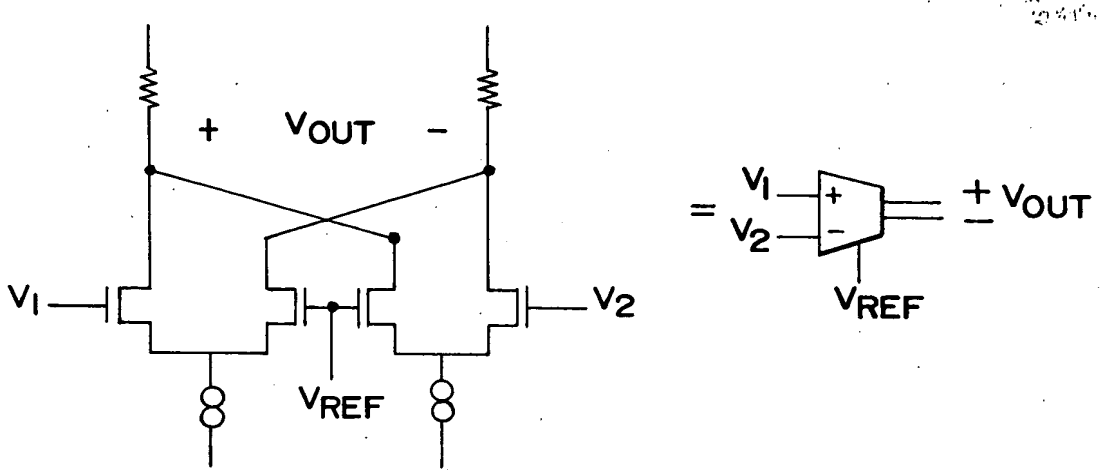


FIG.15B

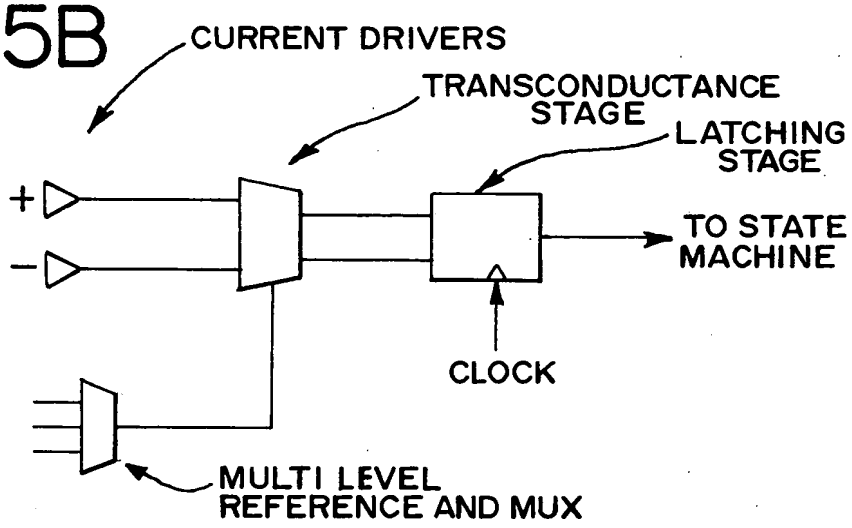


FIG. 16

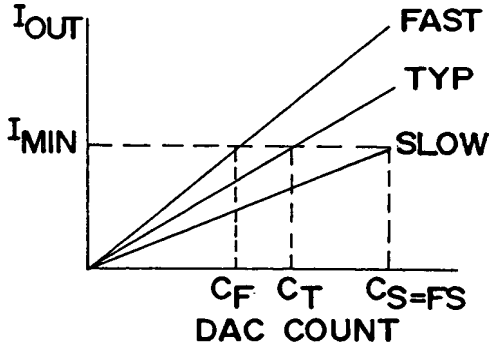
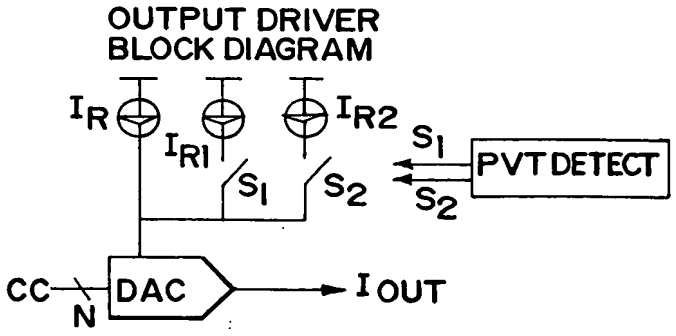


FIG. 17



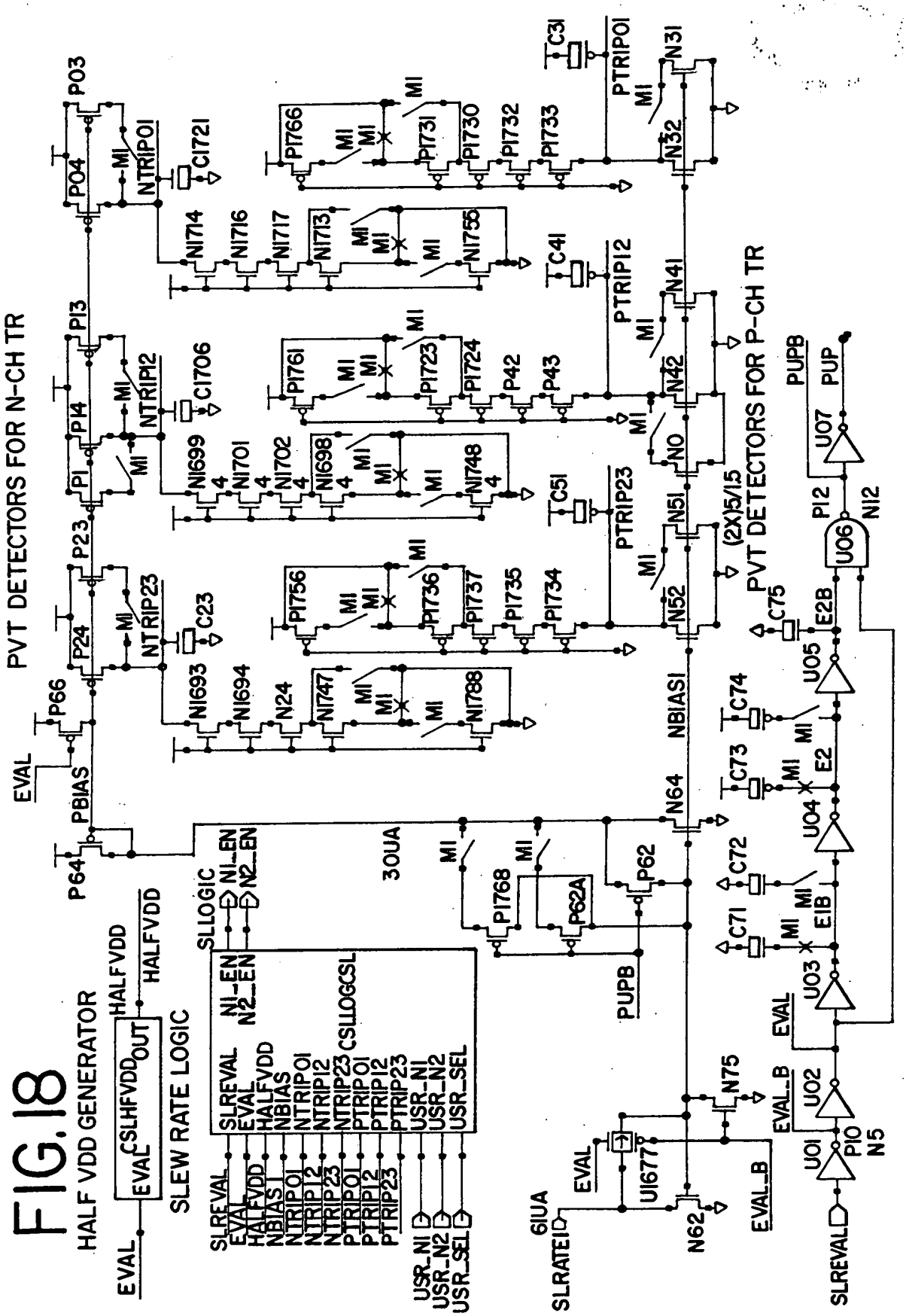


FIG. 18

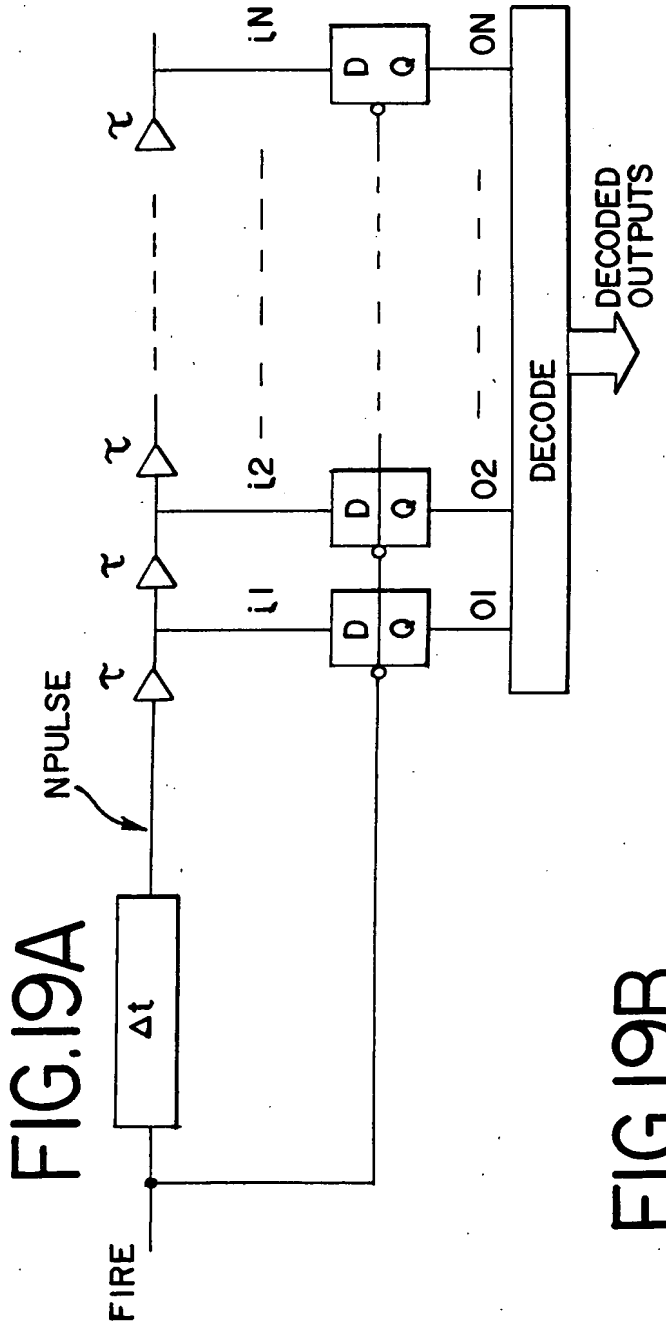


FIG.19A

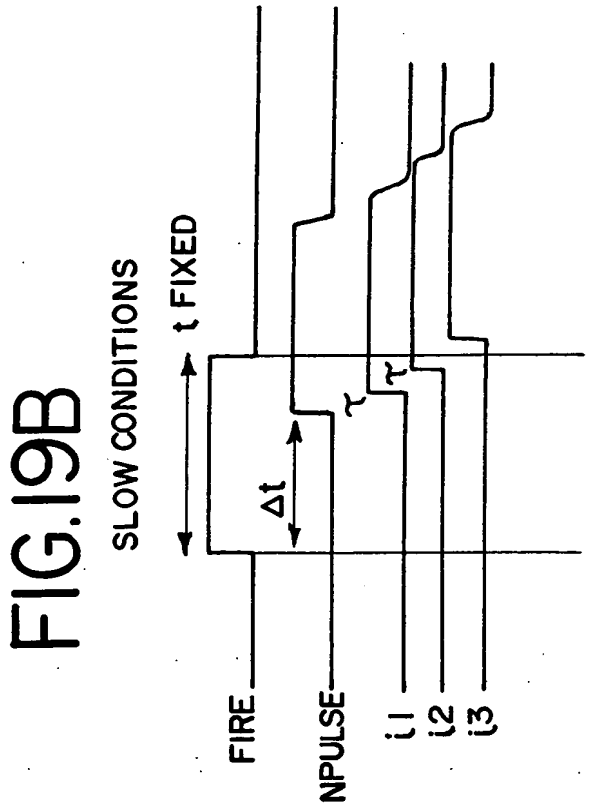


FIG.19B

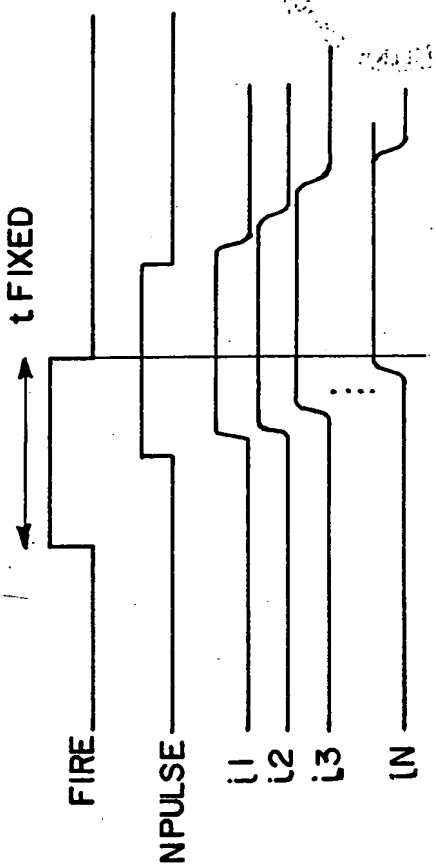


FIG.19C

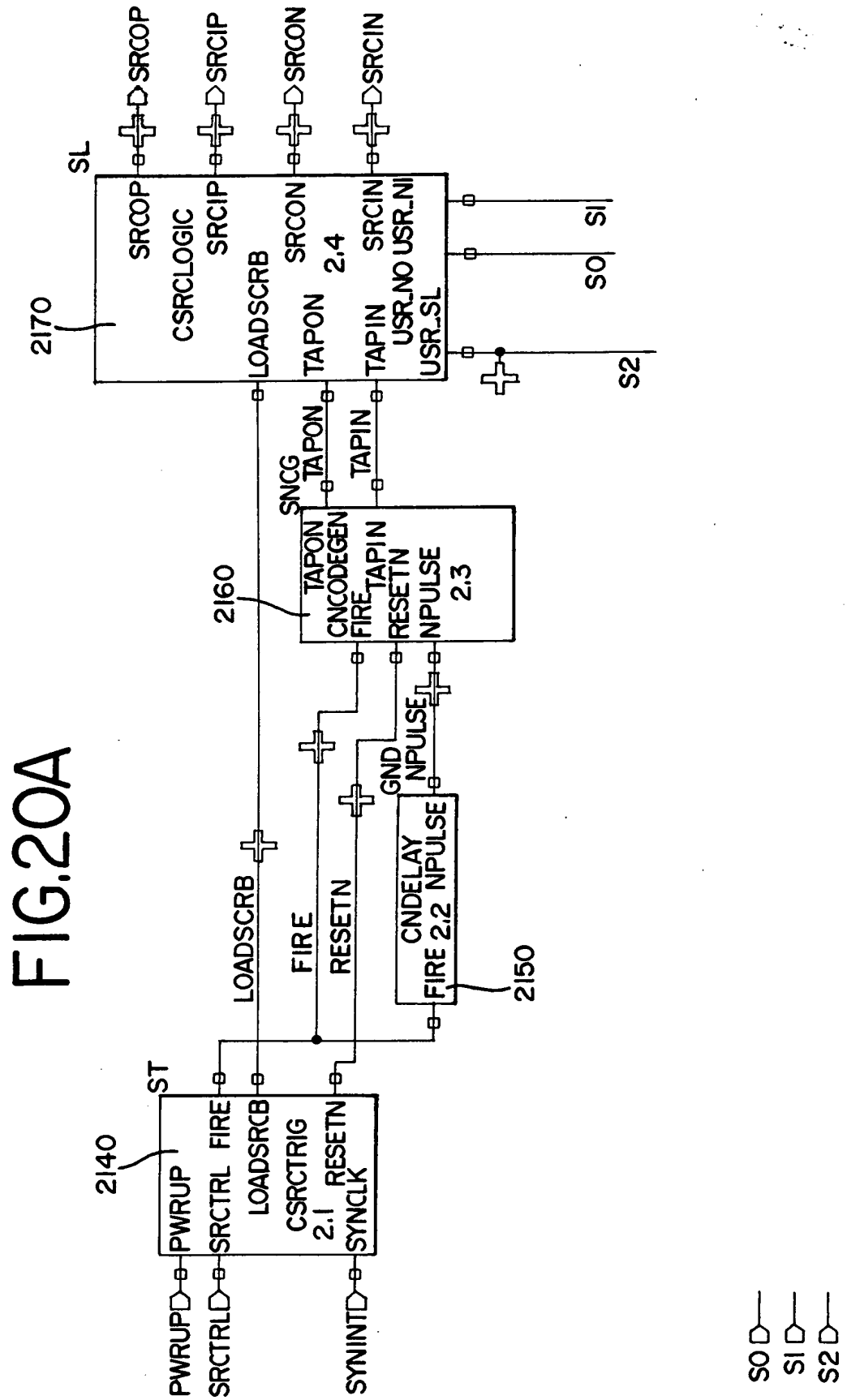


FIG.20A

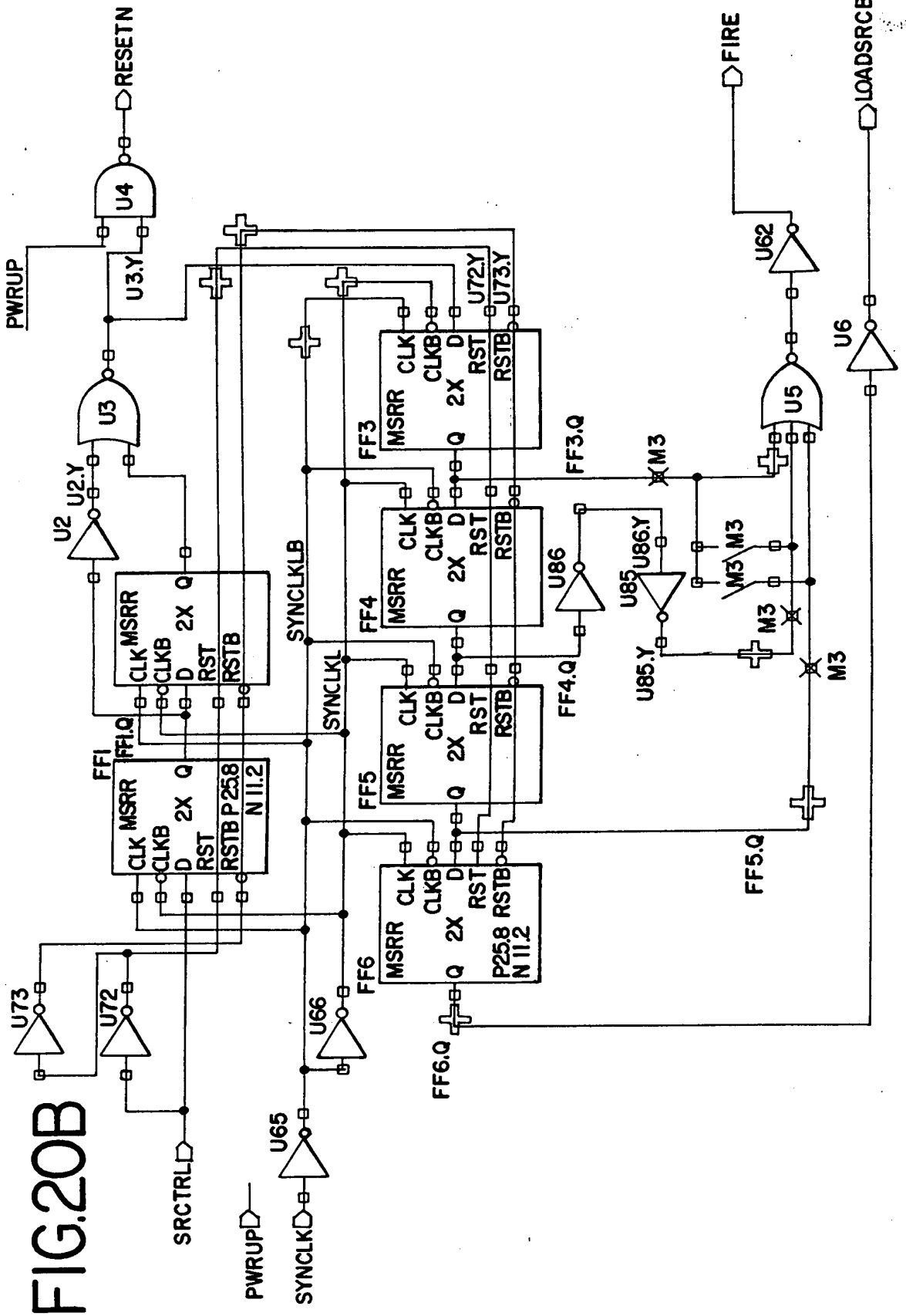


FIG.20B

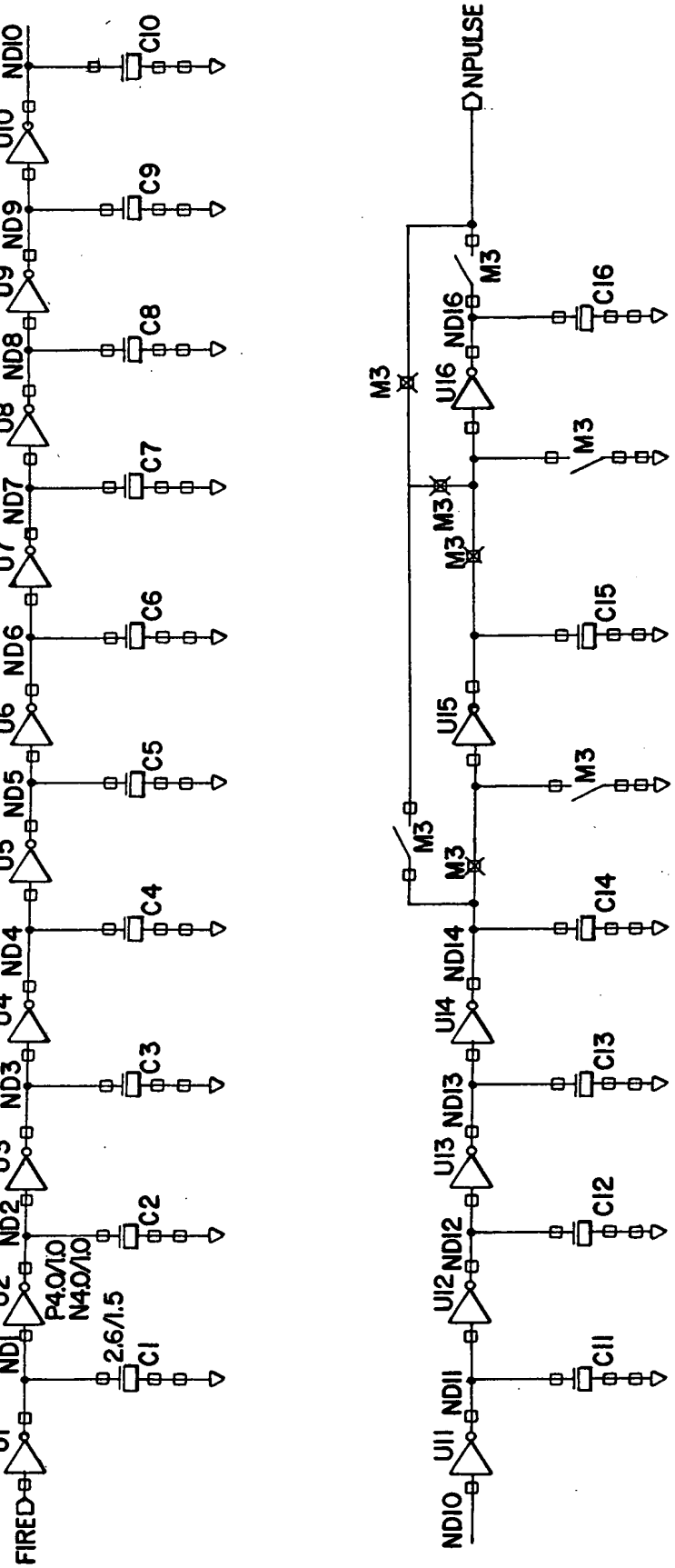


FIG.20C

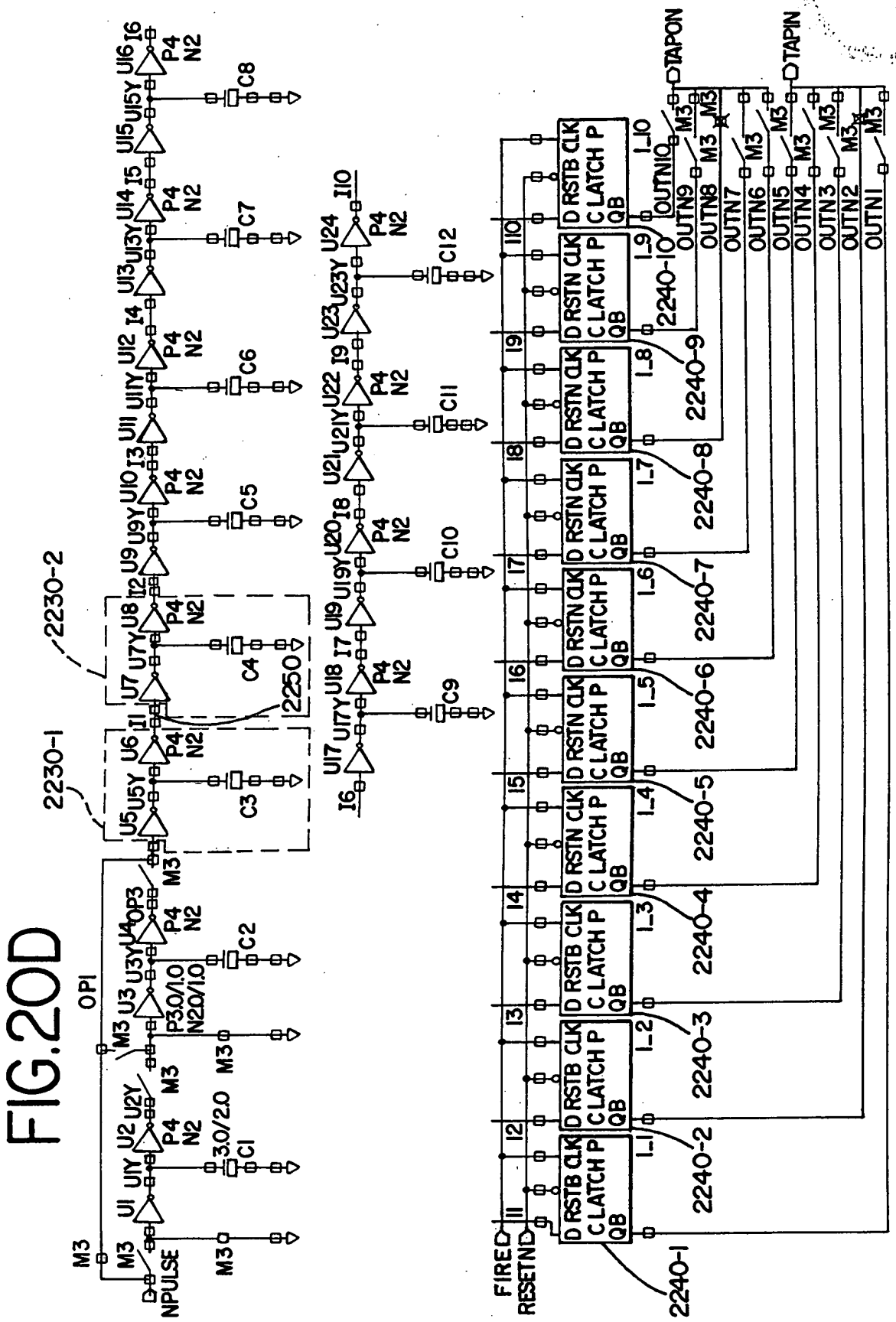


FIG.20D

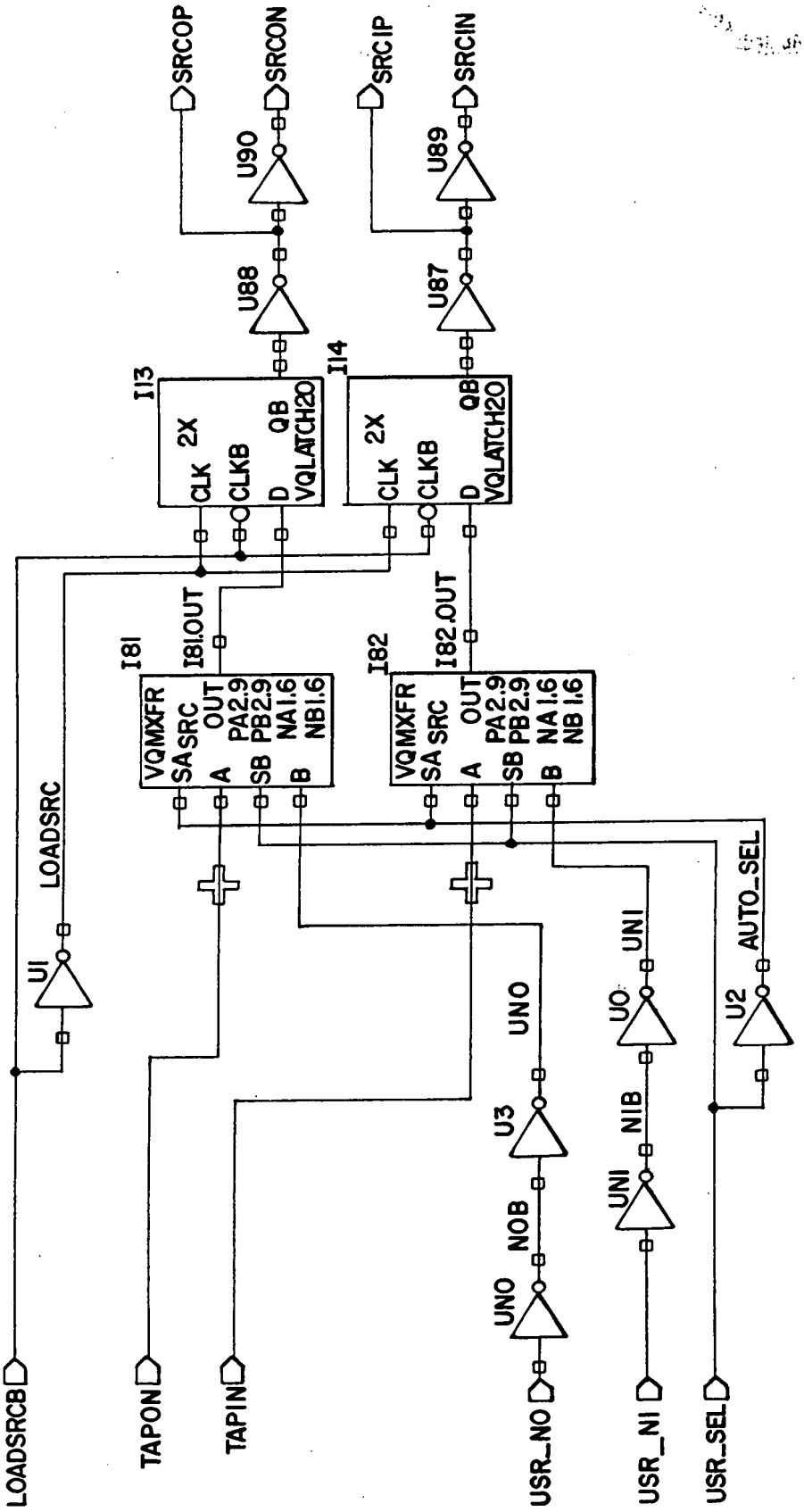


FIG.20E

FIG.21A

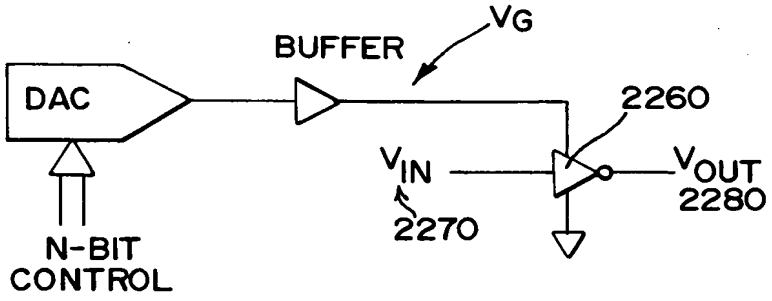


FIG.21B

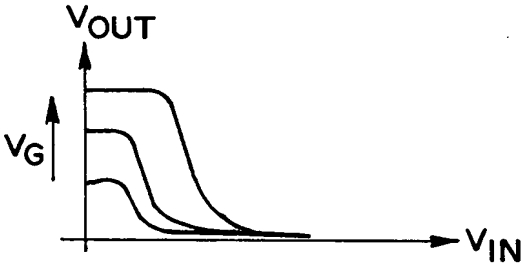


FIG.22

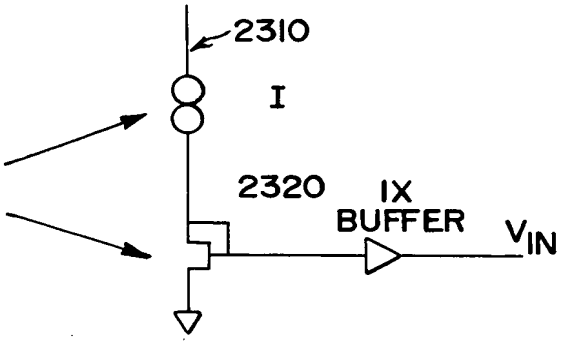


FIG.23

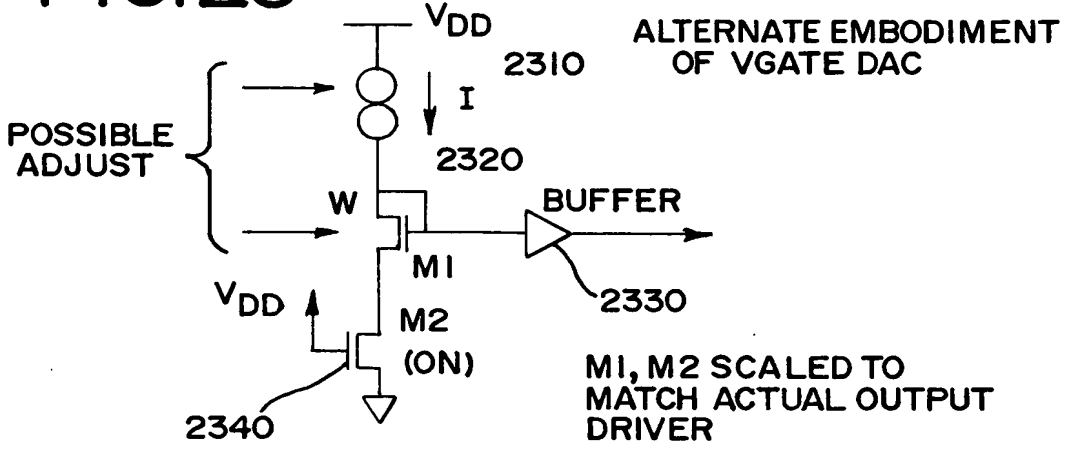
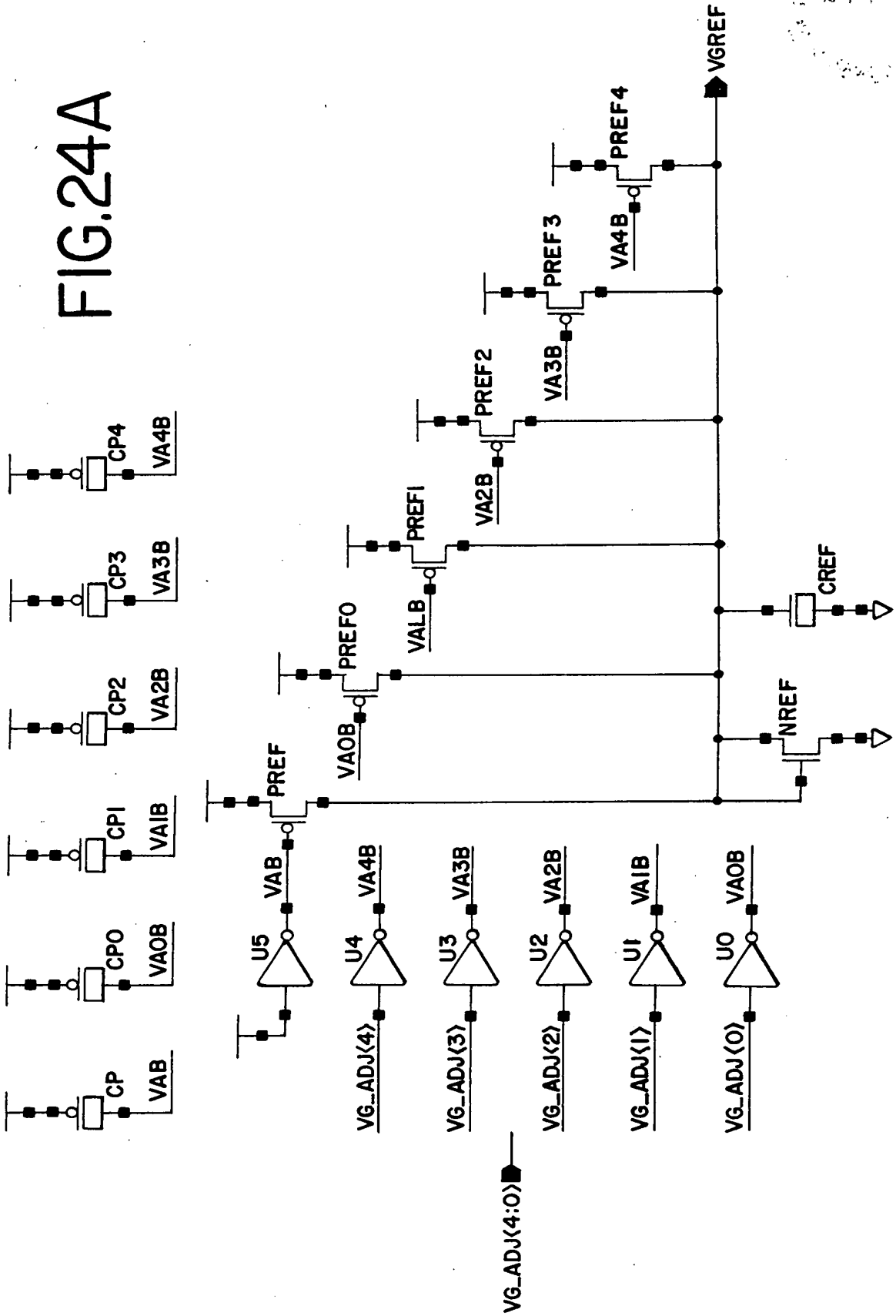


FIG.24A



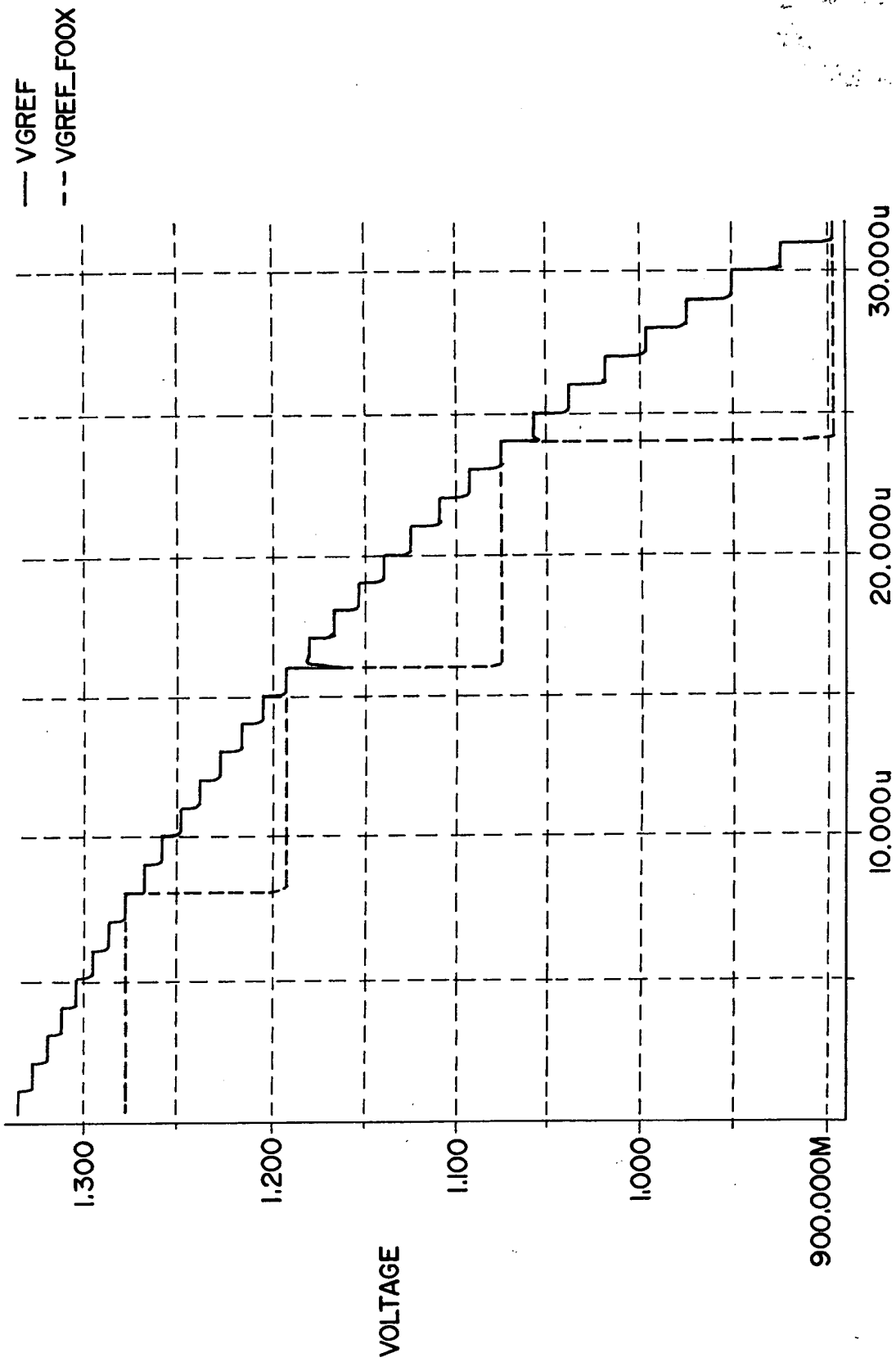

VGREF
VGREF_FOOX
30.000u
20.000u
10.000u
1.300
1.200
1.100
1.000
900.000M
VOLTAGE

FIG.24B